Noise Coupling Due To Through Silicon Vias (TSVs) in 3-D Integrated Circuits

Emre Salman
Department of Electrical and Computer Engineering
Stony Brook University, New York 11794
emre@ece.sunysb.edu

***Abstract*—Three-dimensional (3-D) integration is a promising technology to alleviate the interconnect bottleneck by stacking multiple dies in a monolithic fashion. Both power dissipation and delay can be reduced by utilizing the third dimension where through silicon vias (TSVs) are used for vertical communication. Characteristics of switching noise that couples to a sensitive device due to a TSV are investigated in this paper. A model is developed to evaluate the noise performance of a TSV. Several noise isolation strategies are also discussed. Ignoring noise characteristics during the TSV placement process produces a poor 3-D circuit with high susceptibility to switching noise.**

I. Introduction

Three dimensional (3-D) integration technology is a promising candidate to maintain the benefits of miniaturization by utilizing the vertical dimension rather than decreasing the size of the devices in two dimensions [1]–[3]. The advantages of 3-D integration technology include higher integration density and reduction in the length and number of the global interconnects. These advantages are utilized to reduce the existing gap between logic blocks and memory units in high performance microprocessors. Additional dynamic random access memory can be stacked on top of the processor cores, significantly increasing the memory bandwidth [4]. The application of 3-D integration technology to microprocessors has received significant attention [5], [6].

Another important opportunity provided by 3-D technology is the ability to merge heterogeneous devices for a variety of applications including life sciences [7]. As an example, a monolithic 3-D integrated circuit is depicted in Fig. 1, where each plane serves a dedicated function [1]. Through silicon vias (TSVs) are utilized to achieve communication among the planes. Circuit blocks can be individually optimized based on the required functionality and design objectives. In a conventional transceiver circuitry, digital CMOS technology is typically preferred for data processing units due to higher noise margins and enhanced configurability whereas gallium arsenide based devices are preferred for the front-end blocks such as power amplifier, mixer, voltage controlled oscillator, and low noise amplifier. Furthermore, this communication circuitry can be integrated with a biomedical circuit consisting of, for example, ion-sensitive field effect transistors (ISFETs) [8].

Noise management emerges as a significant limitation in these highly heterogeneous and dense 3-D integrated circuits, as demonstrated in this paper. Several noise coupling mechanisms exist in a 3-D circuit through which switching noise can reach to sensitive analog/RF circuits, degrading the performance. For example, in a typical biomedical application, the input signal of a preamplifier is typically in the range of microvolts [9]. This signal is therefore highly sensitive to switching noise that can couple from the digital signal processing blocks. Noise characteristics within heterogeneous 3-D integrated circuits have not yet received much attention. Noise injected into the substrate by TSVs is investigated in this paper. An electrical model is proposed to estimate the noise that couples to a victim device. Effects of different parameters on peak-to-peak noise are discussed. The efficacy of several noise isolation strategies is also compared.

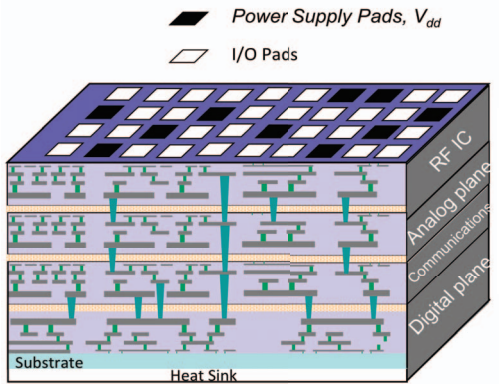

Fig. 1. **Monolithic 3-D integration technology where through silicon vias (TSVs) are utilized to achieve communication among the planes [1].**

II. Interplane Noise Coupling in a 3-D System

As described in the previous section, different circuit functionalities such as digital, analog, and RF can be placed on separate planes in a 3-D integrated circuit. Hence, it is typically assumed that a 3-D circuit has enhanced noise coupling characteristics since each plane has a dedicated substrate. This assumption, however, does not consider the two primary noise coupling paths among the planes:

- Significant noise is injected into the substrate by TSVs that carry signals with high switching activity such as a clock signal.
- Since the power/ground network of several planes is typically shared due to the constraint on the number of pads, simultaneous switching noise propagates across the planes. Furthermore, the substrate of each plane is essentially interconnected since the substrate is biased by the ground network.

978-1-4244-9474-3/11/$26.00 ©2011 IEEE

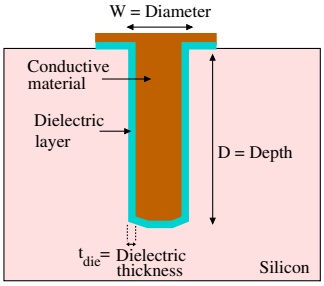

Fig. 2. **Cross section of a through silicon via consisting of a conductive material and a dielectric layer.**

Note that the switching noise that propagates throughout the circuit due to these two mechanisms may reach a sensitive device such as a low noise amplifier, mixer, or oscillator, affecting the device operation and significantly degrading performance. Noise characteristics should therefore be considered during the design process of the power/ground networks and placement of the TSVs. TSV related noise coupling mechanism is investigated in Section II-A. The effect of TSV parameters on noise is discussed in Section II-B. Finally, several 3-D noise isolation strategies are compared in Section II-C.

A. TSV Related Noise Coupling

A typical TSV consists of a metal such as copper or tungsten surrounded by a dielectric layer, as depicted in Fig. 2. The dielectric layer, consisting of TiN or TaN, forms a barrier to prevent the conductive material from diffusing into the silicon [1]. The thickness of this dielectric layer t_{die} is in the range of 0.2 μm to 1 μm [10]. A TSV is typically represented as a cylinder with a diameter W and depth D, as shown in Fig. 2 [11]–[13]. Aspect ratio of a TSV is determined by D/W. These parameters vary depending upon the specific fabrication technology [1]. For typical 3-D technologies, the diameter of a TSV is in the range of 5 μm to 10 μm whereas the depth varies from 50 μm to 100 μm [10].

Noise couples into the substrate when there is a fast signal transition within the TSV. This coupling mechanism is similar to noise coupling into the substrate through source/drain junctions of a transistor. The dielectric capacitance of a TSV, however, is larger as compared to source/drain junction capacitance due to greater dielectric area. TSV related substrate noise coupling is therefore one of the primary noise injection mechanisms in 3-D circuits. An electrical model for this coupling mechanism is depicted in Fig. 3. The TSV is represented by an L shaped, 4-stage distributed RC circuit where the resistance and capacitance represent, respectively, the conductive material and dielectric layer. A resistive substrate model is assumed since the dielectric characteristics are negligible for frequencies below about 10 GHz for a bulk type substrate [14]. The resistance R_{tsv} of the TSV is determined by

$$R_{tsv} = \frac{1}{4}\frac{\rho_c D}{\pi(W/2)^2} = \frac{\rho_c D}{\pi W^2}, \tag{1}$$

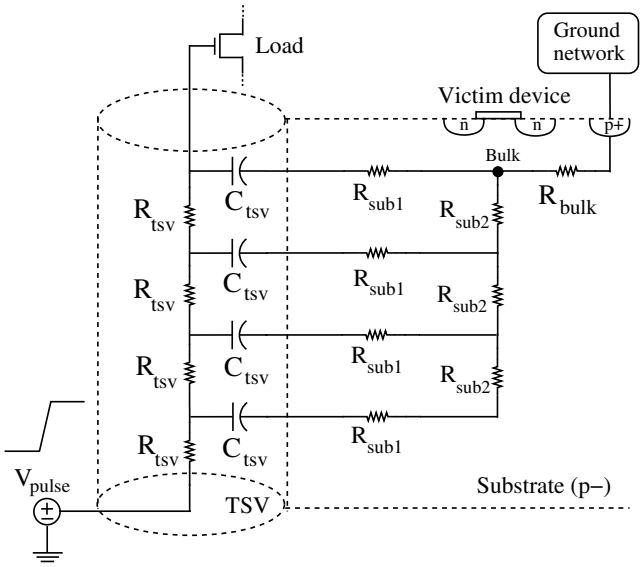

Fig. 3. **Circuit model to represent noise coupling into the substrate by a through silicon via.**

where $\rho_c = 2.8$ $\mu\Omega$cm is the resistivity of the conductive material which is assumed to be copper [12]. The capacitance C_{tsv} due to the dielectric layer is

$$C_{tsv} = \frac{1}{4}\frac{\varepsilon D\pi W}{2t_{die}}, \tag{2}$$

where ε is the dielectric permittivity. Note that half of the sidewall surface area of the cylinder is used to determine the TSV capacitance. The lateral substrate resistance R_{sub1} is determined by

$$R_{sub1} = \frac{\rho_s l}{W(D/4)} = \frac{4\rho_s l}{WD}, \tag{3}$$

where ρ_s is the substrate resistivity and l is the physical distance between the TSV and victim device. A bulk type substrate with $\rho_s = 10$ Ωcm is assumed. Finally, the vertical substrate resistance R_{sub2} is

$$R_{sub2} = \frac{\rho_s(D/4)}{mn} = \frac{\rho_s D}{4mn}, \tag{4}$$

where m and n represent, respectively, the length and width of the victim device. A greater victim size reduces the vertical substrate resistance due to higher cross sectional area.

A pulse voltage source with a specific transition time t_r is connected to the TSV to represent an aggressor digital signal such as clock. The far end node of the TSV drives a capacitive load. The substrate coupling noise that reaches to the bulk node of a victim device is estimated based on these equations and the model illustrated in Fig. 3. For a TSV with W=7.5 μm, D=75 μm, and connected to a clock signal with 100 ps rise/fall times and 1 GHz frequency, the noise at the bulk node is shown in Fig. 4. Note that the ground network is modeled with an RL impedance where the resistance is 2 Ω and inductance is 1 nH. As illustrated in this figure, the peak-to-peak noise voltage that couples to the victim device due to a TSV is

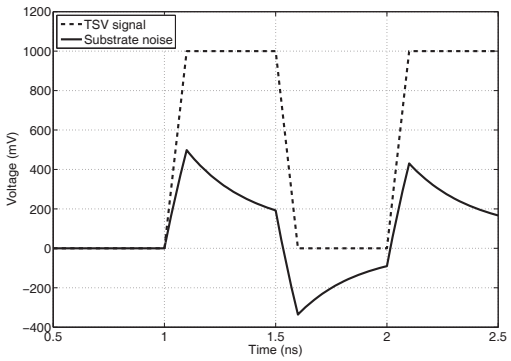

Fig. 4. **Substrate coupling noise at the bulk node of a victim device due to a switching activity within the TSV.**

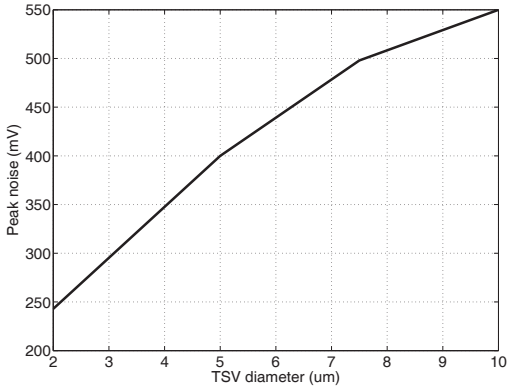

Fig. 5. **Effect of TSV diameter on noise characteristics when TSV depth is equal to 75 μm.**

more than 600 mV when there is no signal isolation. This high noise can significantly degrade the performance of the victim by modifying the threshold voltage due to body effect or may directly couple to the source/drain junctions of the device. The noise coupling characteristics should therefore be considered during the TSV placement process. Considering only thermal constraints may produce a 3-D circuit with poor noise characteristics.

B. Effect of TSV Parameters on Noise

Several parameters such as the depth and diameter of a TSV play an important role in the noise behavior. The TSV depth is primarily dependent upon the wafer thinning capability of the TSV fabrication process. Specifically, a reduced substrate thickness produces a shorter TSV depth. A shorter TSV depth enhances noise characteristics by reducing the TSV capacitance C_{tsv} and increasing the lateral substrate resistance R_{sub1}. Furthermore, a thinner substrate also helps in dissipating the heat, thereby improving thermal stability. Processing thin wafers, however, is a challenging step during fabrication [1].

The effect of TSV diameter on the peak noise is illustrated in Fig. 5. Peak noise is reduced as the TSV diameter is decreased due to a reduction in the TSV capacitance C_{tsv}. Furthermore, lateral substrate resistance is also increased since the TSV behaves as an input port to the substrate. The area of the port is reduced due to a smaller diameter, thereby increasing the substrate resistance.

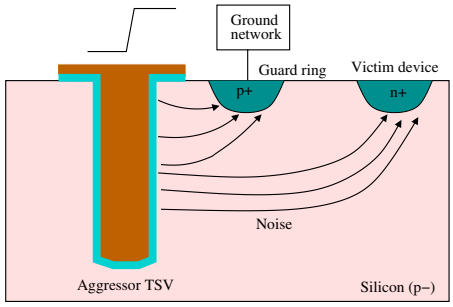

Fig. 6. **Placement of a guard ring near the aggressor TSV to alleviate noise coupling.**

One of the deleterious effects of reducing the TSV diameter is the increase in the TSV resistance. For a data or clock signal, a higher TSV resistance not only increases the *RC* delay, but also causes additional signal attenuation. For a power/ground line, a higher resistance produces greater *IR* drop and reduces the ability of the wire to carry higher current densities which is a primary concern due to electromigration. A tradeoff therefore exists between signal quality/reliability and noise coupling characteristics in determining the TSV diameter. Note that noise coupling can also be reduced by increasing the thickness of the dielectric layer t_{die}. Increasing t_{die} however also increases the TSV resistance since the effective cross sectional area of the conductive material is reduced, assuming the diameter is maintained constant. Several design techniques to achieve higher signal isolation are discussed in the following section.

C. Noise Isolation Strategies

As described in the previous section, significant noise is injected into the substrate by a TSV that carries a high switching activity signal. The magnitude of the noise that reaches to the bulk of a victim device is in the range of half the power supply voltage when there is no noise isolation. The efficiency of two design techniques in reducing TSV related noise coupling is compared in this section. In the first technique, a guard ring is placed around the TSV where the ring dimensions are the same as the victim device, as depicted in Fig. 6.

The guard ring is connected to a quiet ground network not to inject additional noise into the substrate. The impedance of this ground network is assumed to be the same as the impedance of the analog ground network. The circuit model shown in Fig. 3 is modified to consider the effect of a guard ring. Specifically, an additional resistive path to the contact of the ring is included within the substrate to model the guard ring. The guard ring achieves approximately an additional 15 dB isolation. Note that this reduction in noise is relatively independent of the frequency. In the time domain, positive peak substrate noise at the bulk node is reduced from 498 mV to 73 mV. A guard ring biased with a clean ground network is therefore effective in reducing TSV related noise coupling. Guard rings alone, however, are not sufficient since the noise magnitude continues to be significantly high for sensitive circuits. A guard

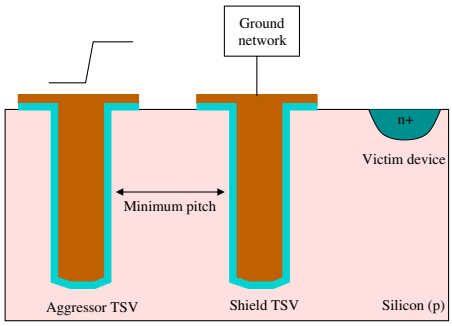

Fig. 7. **Placement of a shield TSV connected to a ground network near an aggressor TSV to alleviate noise coupling.**

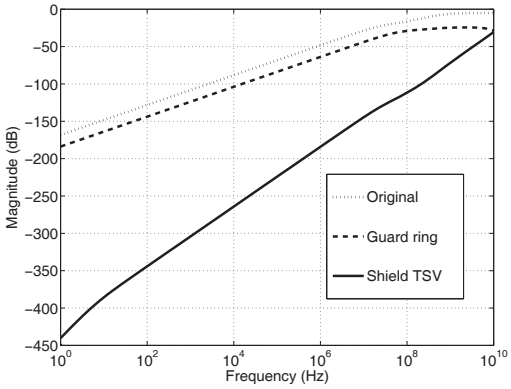

Fig. 8. **Comparison of the three AC responses to evaluate the isolation efficiency of guard rings and TSV shield lines.**

ring can filter the noise current that flows relatively closer to the surface. Alternatively, the noise current injected into the substrate below the surface due to the depth of the TSV can still reach to the victim device, as depicted in Fig. 6.

The second technique is to place another TSV as a shield line, thereby enhancing noise isolation, as depicted in Fig. 7. Note that the TSV shield line is connected to a quiet ground network. The efficiency provided by a TSV shield line in reducing the noise is significantly higher due to additional capacitive isolation. Specifically, a TSV shield line achieves approximately an additional 90 dB isolation at the frequencies in the megahertz range. As the frequency increases to the gigahertz range, the additional isolation provided by the shield TSV is reduced to approximately 30 dB. The AC response of both the guard ring and TSV shield line is shown in Fig. 8. In the time domain, a TSV shield line can reduce the positive peak noise voltage to 22 mV. Transient noise waveforms are compared in Fig. 9 for each case. Note that placing additional TSVs as shield lines is an effective way to reduce substrate noise coupling, particularly at low frequencies. These additional TSVs, however, consume area and reduce the integration density of 3-D circuits due to the minimum pitch between the two TSVs, as illustrated in Fig. 7.

III. Conclusions

TSV related noise coupling mechanism in 3-D integrated circuits has been investigated. The magnitude of the noise that couples to a sensitive victim device due to a signal transition

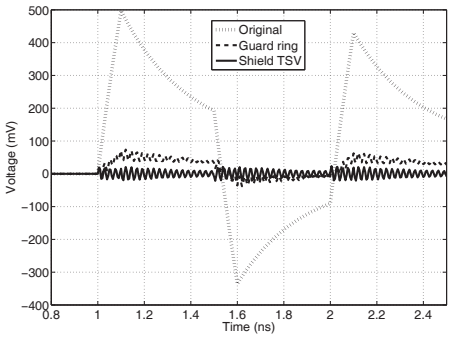

Fig. 9. **Substrate noise waveform at the sense node for three cases: Original circuit with no isolation, use of a guard ring, and use of a TSV shield line.**

within a TSV has been estimated. A circuit model has also been proposed to evaluate noise coupling characteristics. Effect of several parameters such as TSV depth and diameter on noise characteristics has been analyzed. Finally, the amount of noise that can be reduced by using a guard ring and TSV shield line has been compared.

References

[1] V. F. Pavlidis and E. G. Friedman, *Three-Dimensional Integrated Circuit Design*, Morgan Kaufmann, 2009.

[2] V. F. Pavlidis and E. G. Friedman, "Interconnect-Based Design Methodologies for Three-Dimensional Integrated Circuits," *Proceedings of the IEEE*, Vol. 97, No. 1, pp. 123–140, January 2009.

[3] R. J. Gutmann *et al.*, "Three-dimensional (3D) ICs: A technology platform for integrated systems and opportunities for new polymeric adhesives," *IEEE International Conference on Polymers and Adhesives in Microelectronics and Photonics*, pp. 173–180, October 2001.

[4] A. W. Topol *et al.*, "Three-dimensional Integrated Circuits," *IBM Journal of Research and Development*, Vol. 50, No. 4/5, pp. 491–506, July/September 2006.

[5] B. Vaidyanathan *et al.*, "Architecting Microprocessor Components in 3D Design Space," *International Conference on VLSI Design*, pp. 103–108, February 2007.

[6] G. H. Loh and Y. Xie, "3-D Stacked Microprocessor: Are We There Yet?," *IEEE Micro*, Vol. 30, No. 3, pp. 60–64, May/June 2010.

[7] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and Systems-on-Chip Integration," *Proceedings of the IEEE*, Vol. 89, No. 5, pp. 602–633, May 2001.

[8] B. Palan *et al.*, "New ISFET Sensor Interface Circuit for Biomedical Applications," *Sensors and Actuators B*, Vol. 57, No. 1/3, pp. 63–68, September 1999.

[9] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow-Power Electronics for Biomedical Applications," *Annual Review Biomedical Engineering*, Vol. 10, pp. 247–274, April 2008.

[10] S. Ramaswami *et al.*, "Process Integration Considerations for 300 mm TSV Manufacturing," *IEEE Transactions on Device and Materials Reliability*, Vol. 9, No. 4, pp. 524–528, December 2009.

[11] D. Henry *et al.*, "Low Electrical Resistance Silicon Through Vias: Technology and Characterization," *Proceedings of the IEEE Electronics Components and Technology Conference*, pp. 1360–1366, May/June 2006.

[12] C. A. Bower *et al.*, "High Density Vertical Interconnects for 3-D Integration of Silicon Integrated Circuits," *Proceedings of the IEEE Electronics Components and Technology Conference*, pp. 399–403, May/June 2006.

[13] D. M. Jang *et al.*, "Development and Evaluation of 3-D SiP with Vertically Interconnected Through Silicon Vias (TSV)," *Proceedings of the IEEE Electronics Components and Technology Conference*, pp. 847–852, May/June 2007.

[14] H. Lan, Z. Yu, and R. W. Dutton, "A CAD-oriented Modeling Approach of Frequency-Dependent Behavior of Substrate Noise Coupling for Mixed-Signal IC Design," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 195–200, March 2003.