Impact of Low-Doped Substrate Areas on The Reliability of Circuits Subject to EFT Events

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Abstract—**External stresses, such as those generated due to Electrical Fast Transient (EFT) events, generate over-voltages which may result in reliability failures at the IC level either in the form of recoverable or permanent damage of the IC. In the present paper, the relationship between the technology characteristics within a design framework and the permanent failures that such an EFT event can produce are discussed. Solutions to minimize the impact of such EFT events are presented.**

I. Introduction

The burst of over-voltage pulses characterizing an EFT event [1] is generally associated with external turn-on/turn-off or switching events such as those of relays of inductive/capacitive loads and electrical motors [2]. Over-voltages are generated on the external cables, propagating to any connected electronic component. The impact of these pulses on an IC can be observed as electrical failure by means of such mechanisms as breakdown and latch-up [3, 4]. The protection against such over-voltages is required to be implemented predominantly at the IC level, since board-level solutions generally add noticeably to the cost of the final application. I/O level clamp circuits can protect the circuit against such over-voltages [3, 5], while latch-up rules can improve circuit latch-up immunity.

Technology options may have consequences such as a greater susceptibility to EFT related over-voltages, which may require design changes to preserve a robust solution in this environment. The relationship between technology and IC reliability when the IC is subject to EFT induced over-voltages is the focus of this paper. Specifically, the focus is on EFT-induced device breakdown.

The remainder of the paper is organized as follows. The IC environment for the subject reliability issue is presented in Section II. Results are described in Section III. The paper is concluded in Section IV.

II. Synopsis

Low-doped substrate areas represent a technology option for technologies supporting high voltage devices. Such high-voltage devices are used in various blocks across the IC, including the I/O pads. Since the I/O pads represent the interface with the outside world, devices in pad circuits are most prone to be affected by occurrences like the over-voltages generated by EFT events.

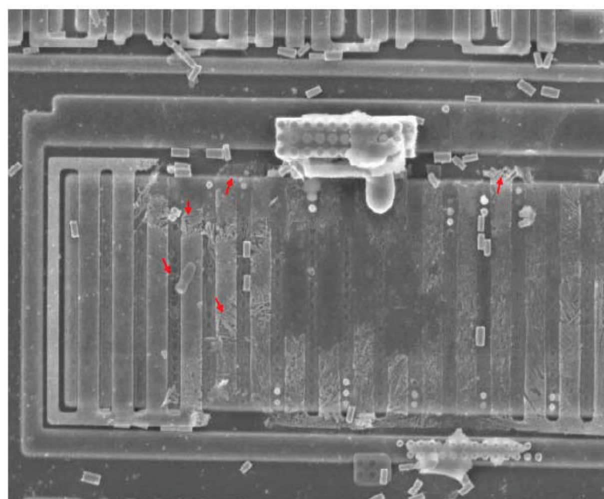

Fig. 1. EFT induced device failure

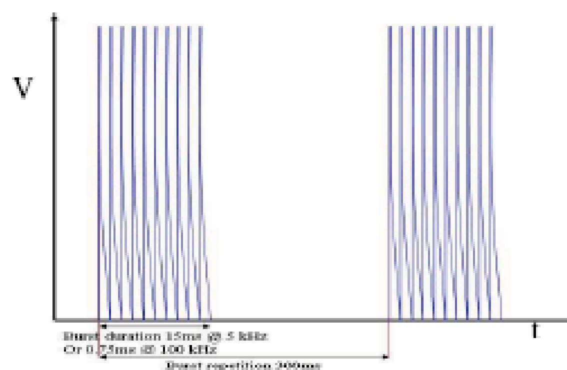

Fig. 2. EFT pulse burst. Burst duration 15ms@5KHz or 0.75ms@100KHz, with burst repetition of 300ms.

Protection circuits, including clamps, are designed to protect the I/Os. However, during the over-voltage bursts of an EFT event, transients lead to

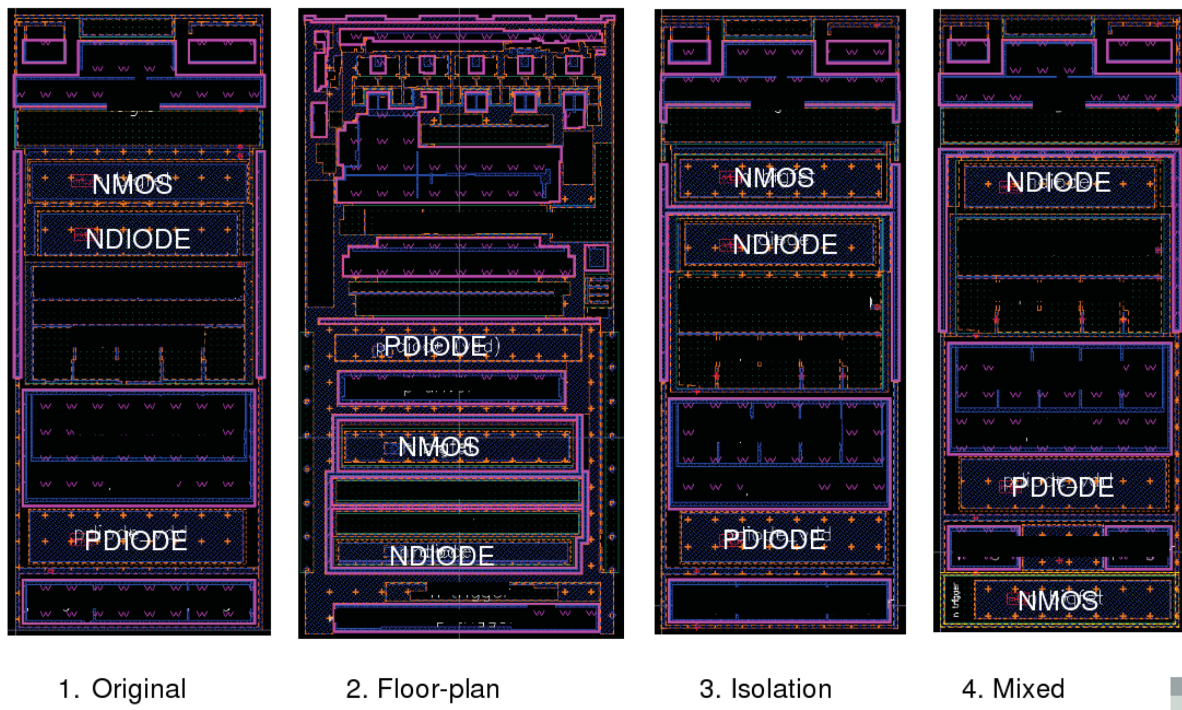

Fig. 3. Layout models of the I/O pad: initial version and improvements

forward bias of device junctions resulting in injection of large substrate currents. In the absence of isolation options such as triple-wells, these transient substrate currents can flow anywhere across the chip. If these substrate currents are not sunk efficiently into the ground domains of the chip, they can affect the breakdown voltage of devices, and lead to device failure as shown in Fig. 1.

During IC characterization measurements, the burst is generated according to the IEC standard [1], as shown in Fig. 2. The I/O pads under observation feature ESD protection. The back-to-back ESD diodes undergo transient forward-bias during the EFT burst.

III. Discussions and Results

The first step in demonstrating the synopsis described in Section II is by analyzing the circuit and layout of the I/O pad where the failure occurs. The initial layout is depicted on the left side of Fig. 3. The other three layouts in Fig. 3 represent recommended improvements of the initial layout. The improvements consist in repositioning NMOS and Diode for increased distance, and inserting isolation between the two devices for improved substrate current sink and dispersion. It is important that, in the initial layout, the ESD NDIODE is in the same low-doped substrate area as the large high-voltage NMOS.

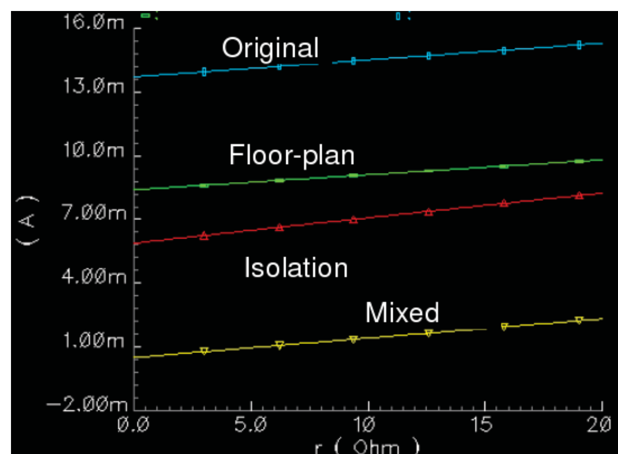

Fig. 4. Comparative results of the four layout versions

Based on the concepts discussed in Section II, several layout options are being designed. From left to right in Fig. 3, these are:

1. Original layout (Original)
2. NMOS and diode within a different floor-plan (Floor-plan)
3. NMOS and diode with substrate contacts in a more highly-doped substrate region instead of the low-doped substrate region in the original layout (Isolation)

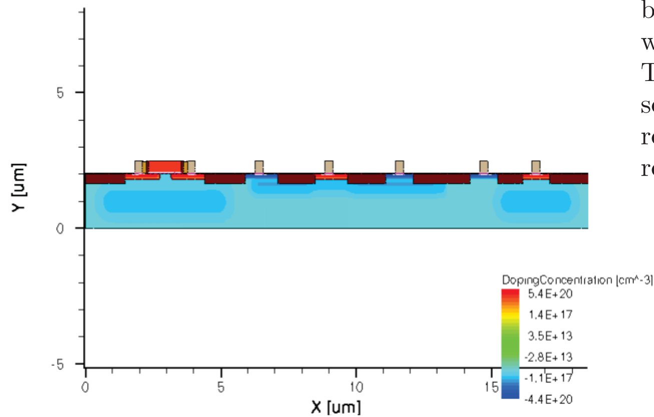

Fig. 5. 2D TCAD setup example. The "Isolation" case is depicted, with the NMOS on the left, NDIODE on the right.

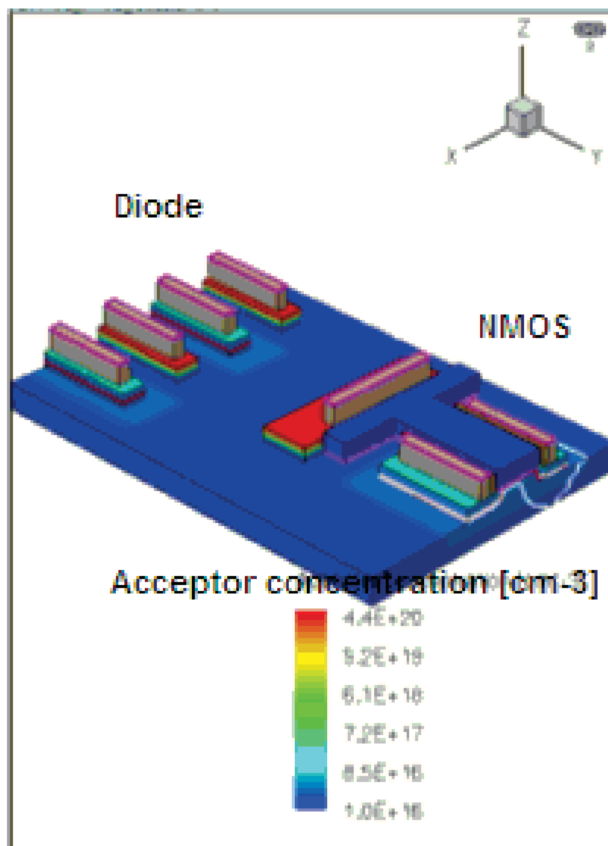

Fig. 6. 3D TCAD setup example. The "Original" case is depicted, with the NMOS and the NDIODE.

4. A combination of (2) and (3) above ((3) with a greater distance between the NMOS and diode) (Mixed)

After extracting the substrate parasitics in each of the four cases, a comparative analysis is performed by injecting a reference current at the diode location while observing the current at the NMOS location. The results are depicted in Fig. 4. The currents observed at the NMOS are shown to be progressively reduced with every successive improvement. These results are summarized in Table I.

TABLE I

CURRENT OBSERVED AT NMOS VS. LAYOUT OPTION

No.	Layout	Approx. current at NMOS (mA)
1	Original	14
2	Floor-plan	8
3	Isolation	5.5
4	Mixed	< 1

To make the correspondence between the substrate currents observed at the NMOS and the breakdown voltage of this device, comparative 2D and 3D TCAD simulations are performed. Structures were built by dropping 1D implant simulations into a 2D and 3D framework using a lateral factor of 0.8. Device simulations were done using drift diffusion. Some simple calibration of threshold and current to measured data was done. Examples of 2D and 3D structures are shown in Figs. 5 and 6.

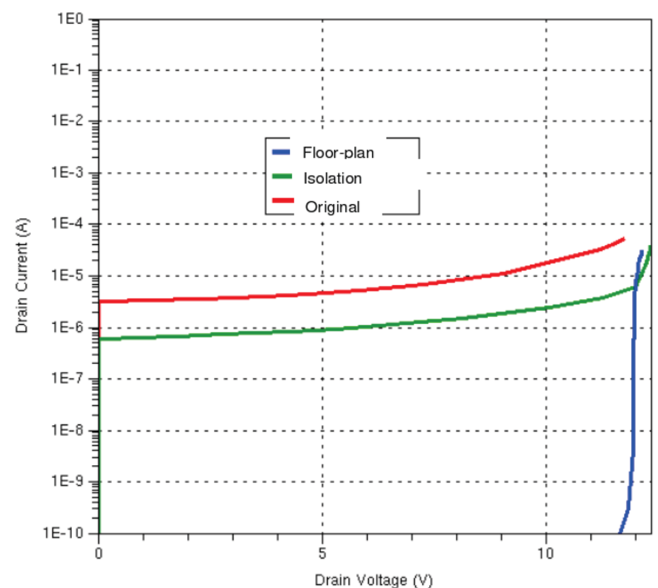

Fig. 7. Comparative results of breakdown voltage for three layout versions

The TCAD results demonstrate the correlation between the increased substrate current at the NMOS and the corresponding decrease in the breakdown voltage observed for that device, as shown in Fig. 7. The corresponding measured data when the diode is

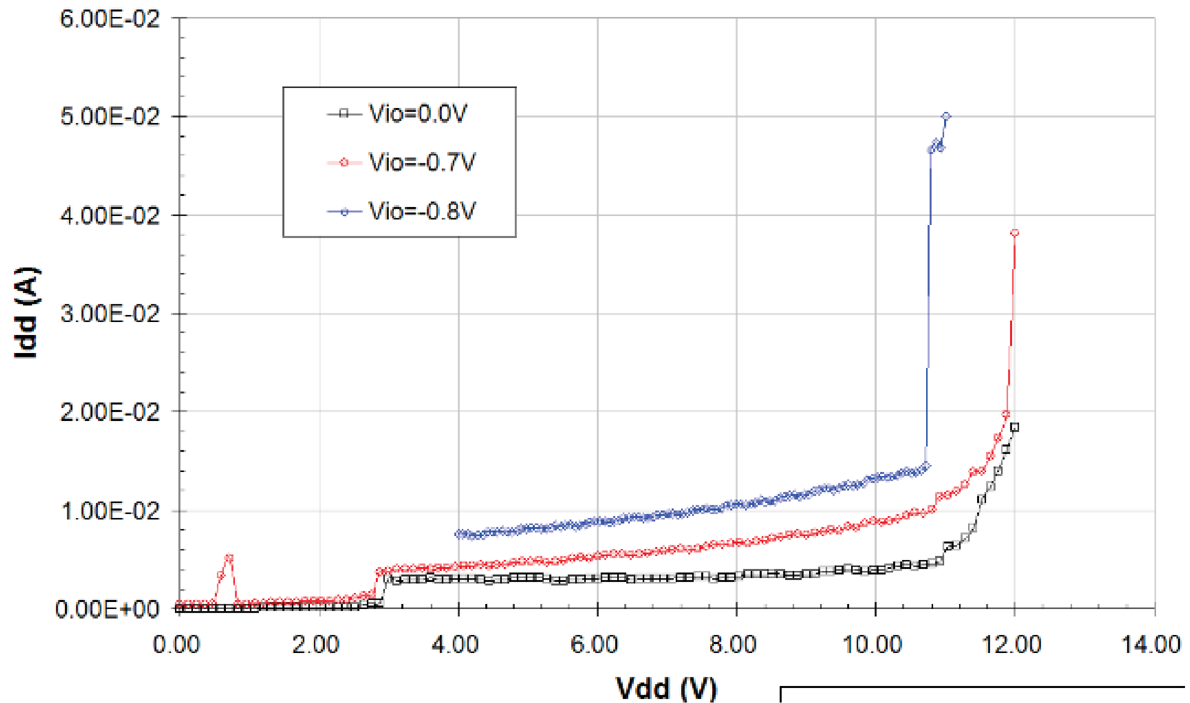

Fig. 8. Variation of NMOS breakdown voltage with the diode forward bias voltage

increasingly forward biased is shown in Fig. 8.

For layouts with greater isolation the drain voltage where the NMOS drain current goes vertical (indicating breakdown) is increased in both simulation and measured data.

IV. Conclusions

Solutions for improved IC reliability when subject to EFT events have been demonstrated. The relationship between the substrate currents and the breakdown of devices is shown to be the main cause of the reliability degradation. The solutions represent a direct consequence of reducing the substrate currents. It is demonstrated that reliability improvements can be achieved by means of a considerate floor-plan and careful considerations of the technology-offered process options.

References

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