Compact Substrate Models For Efficient Noise Coupling and Signal Isolation Analysis

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Abstract— **Current propagation within a lightly doped substrate is approximated with a half-ellipse to efficiently estimate substrate resistances. As opposed to existing work, the proposed model contains only one fitting parameter. Compact models are also developed to determine the isolation efficiency of several commonly used structures such as a guard ring and triple well. The accuracy of these models is verified by comparing the models with a commercial substrate extraction tool based on a boundary element method. These models are used to compare several isolation structures within an industrial mixed-signal circuit with a lightly doped substrate.**

I. Introduction

Substrate noise coupling continues to be a primary concern in highly heterogeneous mixed-signal circuits such as transceivers where digital and analog/RF functions are placed on the same monolithic substrate [1]. The demand for higher integration exacerbates this issue due to the reduced physical distance between the aggressor digital and sensitive analog/RF blocks.

A variety of noise reduction and isolation techniques exist to alleviate substrate noise coupling. The evaluation of these techniques and quantification of the substrate noise at the boundary of the sensitive circuit require a computationally efficient analysis methodology which simultaneously considers the circuit activity, power/ground network, and substrate network.

Existing substrate network extraction techniques fail when analyzing large scale circuits due to increasing computational complexity, making the efficient estimation of the substrate noise prohibitive. Current approaches to model the substrate can typically be divided into two classes. The first class includes those techniques that discretize the substrate into a 3-D $R(C)$ mesh to determine the impedances such as the finite difference method (FDM) [2], [3] and the boundary element method (BEM) [4], [5]. Although highly accurate, the primary limitation of these approaches is the increase in computational complexity with the size of the circuit, prohibiting the efficient analysis of large scale mixed-signal circuits [6].

The second class of substrate modeling methods is the use of macromodels to represent the impedance between two ports on a substrate [7], [8], [9]. The primary advantage of these approaches is fast estimation of the substrate impedance with reasonable accuracy, supporting the efficient evaluation of several isolation structures without extracting the entire substrate. The difficulty in using these models is the requirement to fit several process dependent parameters. Compact models are developed in this paper that require *only one* fitting parameter as opposed to multiple parameters as proposed in existing work [7], [8], [9]. Furthermore, these new models are applicable to a lightly doped substrate which is more challenging to model [10], but are commonly used in mixed-signal and analog circuits due to enhanced isolation [8], [11]. Note that the majority of existing models is valid only for a heavily doped substrate [7], [9], [12], [13]. where the bulk can be represented as a single equipotential node [10].

The rest of the paper is organized as follows. The proposed models to efficiently estimate the substrate resistances are described in Section II. These models are also used to evaluate the isolation efficiency of several structures such as a guard ring and triple well. An industrial circuit with a lightly doped substrate is used to compare the common isolation structures, as described in Section III. The paper is concluded in Section IV.

II. Proposed Substrate Models

Several models to efficiently estimate the substrate resistances are described in this section. The proposed half-ellipse model to determine the substrate resistance between two ports is described in Section II-A. Models are also developed for several commonly used signal isolation structures. Specifically, a circuit model for a guard ring and a triple-well with guard ring structure is described, respectively, in Sections II-B and II-C. Note that a lightly doped (bulk type) substrate is assumed for these models due to two reasons: (1) a model of a bulk type substrate is significantly more complicated than an epi type substrate since the bulk cannot be represented as a single equipotential node, and (2) a bulk type substrate is more appropriate for mixed-signal and analog circuits where substrate coupling is of primary concern.

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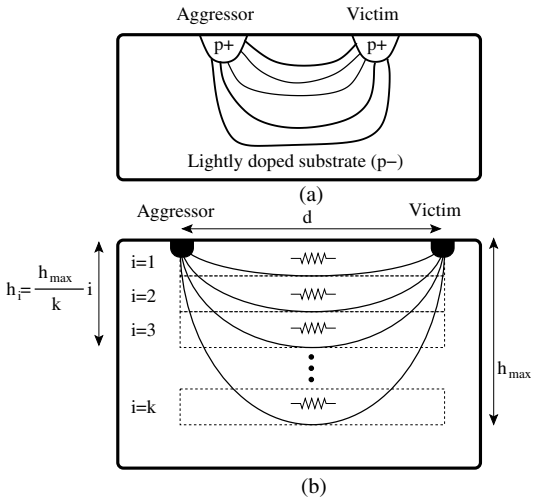

Fig. 1. Current propagation between two ports within a lightly doped substrate: (a) based on experimental and device simulations, (b) approximation based on the half-ellipse model.

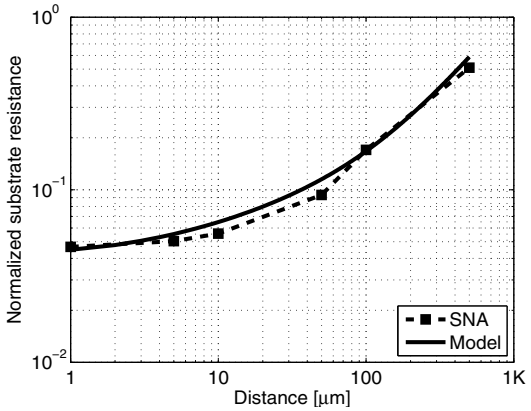

Fig. 2. Comparison of the model with a commercial substrate extraction tool (SNA). Proposed model accurately captures the nonlinear dependence of the substrate resistance with distance.

A. Substrate Resistance Between Two Ports

Current propagation between two ports, *e.g.*, an aggressor and victim, within a lightly doped substrate is depicted in Fig. 1(a) [14]. A large portion of the current flows near the surface, but a smaller portion of the current flows deeper within the substrate. The resistance of these deeper paths is therefore higher than those paths near the surface. This current flow is approximated with a *half-ellipse*, as depicted in Fig. 1(b). The perimeter of an ellipse is used to estimate the resistance of the path. Since the perimeter of the half ellipse is greater within the deeper parts of the substrate, as shown in Fig. 1(b), the substrate resistance is also greater in the proposed model.

Each half-ellipse shown in Fig. 1(b) represents a current path, and therefore, is modeled as a substrate resistance. The value of each resistance is based on the perimeter P of the half-ellipse [15],

$$P(d,h_i) = \frac{\pi}{2}\left[3\,(0.5d+h_i) - \sqrt{(1.5d+h_i)\,(0.5d+3h_i)}\right], \quad (1)$$

where the dimensions d and h_i are illustrated in Fig. 1(b). Note that these dimensions are proportional to the two radii of the half-ellipse. d is constant for each path, but h_i varies based on the depth of the current. The resistance R_i of each path is approximated using (1) as

$$R_i = \rho \frac{P(d,h_i)}{(h_{max}/k)w}, \quad (2)$$

where ρ is the resistivity of the substrate, w is the width of the port, and k determines the number of vertical substrate resistances within the model. A higher k produces a more accurate result at the expense of a linear increase in computation. The results presented in this paper are obtained with $k = 100$. h_{max} is a technology dependent fitting parameter that determines the depth of the current within the substrate. Finally, the effective resistance R_{eff} between two ports is the sum of the parallel resistors,

$$R_{eff} = \frac{1}{\left(\sum_{i=1}^{k} \frac{1}{R_i}\right)}. \quad (3)$$

The proposed half-ellipse based model is compared with SubstrateStorm, a commercial BEM based substrate extraction tool, also referred to as SNA [16]. This comparison is illustrated in Fig. 2 to evaluate the accuracy of the model. The normalized substrate resistance between two ports is shown in this figure as a function of the distance between these ports. Note that the model accurately captures the nonlinear dependence of the substrate resistance over a wide range of distance, where the RMS error is 14%.

B. Guard Ring Isolation

A guard ring refers to the p+ substrate contacts (or n+ taps for the N-well) placed around the aggressor or victim and connected to a ground pad (or power pad for the N-well), as illustrated in Figs. 3(a) and (b). The guard ring eliminates noise coupling by providing a low impedance path for the injected noise current within the substrate (or N-well), thereby improving the noise characteristics of the victim. Note that a guard ring can be placed around only the aggressor, victim, or both the aggressor and victim.

The proposed circuit model of a guard ring is depicted in Fig. 3(c). Resistors R_1 to R_4 represent the substrate resistance from the noise source to the ring. These resistances are determined using the model described in Section II-A. R_5 to R_8 represent the resistance of the metal surrounding the ring. These resistances can be determined from the sheet resistance since the width and length of the metal is known. The impedance between the ring and ground pad is modeled by Z_{gnd}. Finally, the substrate resistance between the ring and victim is represented by R_{sub} which is determined by (1) and (2).

Several parameters such as the width and connectivity of the ring and pad location significantly affect the overall efficiency of the ring. For example, the isolation achieved by a ring is

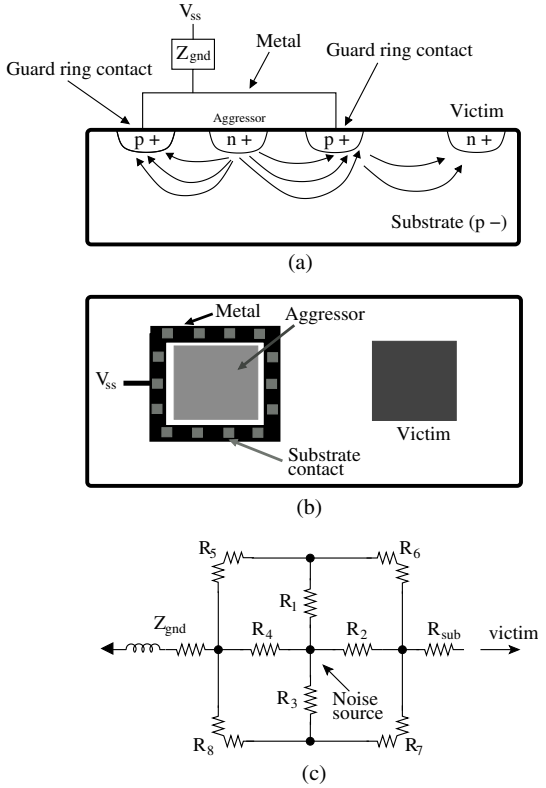

Fig. 3. Illustration of a guard ring: (a) cross-sectional view, (b) top view, (c) proposed circuit level description.

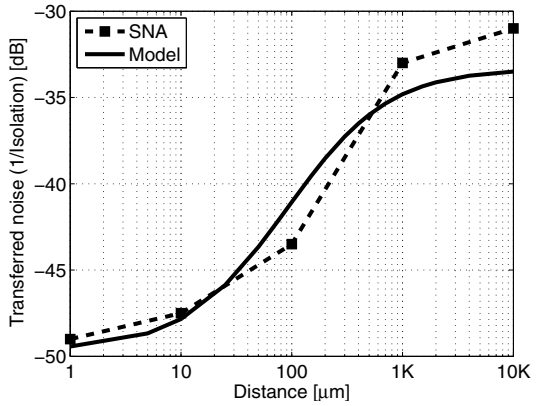

Fig. 4. Magnitude of transferred noise as a function of the distance between the ring and ground pad.

illustrated in Fig. 4 as a function of the distance between the ring and ground pad. As shown in this figure, the proposed model exhibits reasonable accuracy as compared to SNA. Note that as the distance between the ring and ground pad increases, the isolation degrades due to the higher impedance Z_{gnd} of the ground network. The impedance of the ground network connected to the ring should therefore be lower to increase the efficiency of the ring.

C. Triple Well with Guard Ring

Another technique to further increase the isolation efficiency of a guard ring is to use a deep n-well, also referred to as a triple well or isolated p-well, as illustrated in Fig. 5(a). The efficiency is increased by the junction capacitances C_{j1} and C_{j2}, as shown in this figure. The proposed circuit model of a triple well with a guard ring is depicted in Fig. 5(b). The model is similar to the guard ring model with the addition of the junction capacitances. The junction between the isolated p-well and deep n-well is represented with four capacitances (C_{j1}) and the junction between the deep n-well and p-well is represented by the capacitance C_{j2}. These capacitances are determined based on the dimensions of the deep n-well and certain technology parameters. Note that the substrate resistances R_1 to R_4 and R_{sub} are determined as described in Section II-A.

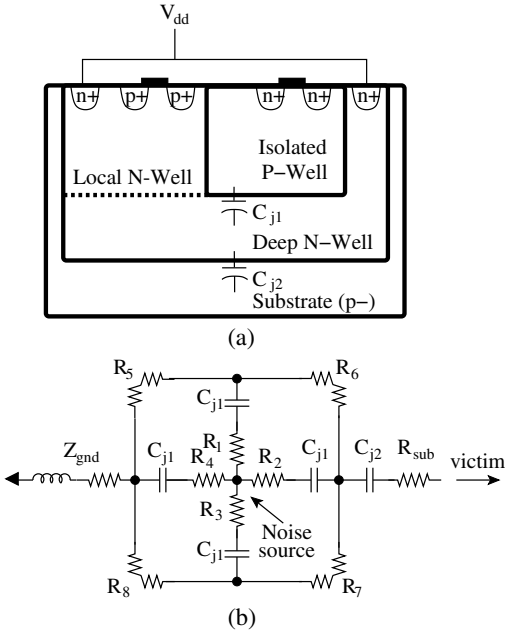

Fig. 5. Triple well structure to further increase the efficiency of a guard ring: (a) cross-sectional view, (b) proposed circuit level description.

The isolation obtained with a triple well with a guard ring is compared with SNA in Fig. 6 for several circuit sizes at two different frequencies. The proposed model accurately captures the effect of circuit size on noise isolation, as illustrated in this figure. Note that the isolation efficiency is significantly reduced at a higher frequency since the effect of the capacitances diminishes as the frequency increases. Also note that the isolation efficiency of the triple well structure is degraded as the size of the aggressor circuit grows although the amount of noise injection is the same. This result is due to the increasing junction capacitances within a larger circuit, also demonstrated in [17]. It is therefore desirable to divide a large deep n-well into smaller sections to improve the efficiency of the isolation.

III. Discussion

The isolation obtained in several different configurations are compared in this section using the proposed models. Specifically, five cases are compared for the same industrial mixed-signal circuit in a 90 nm CMOS technology with a

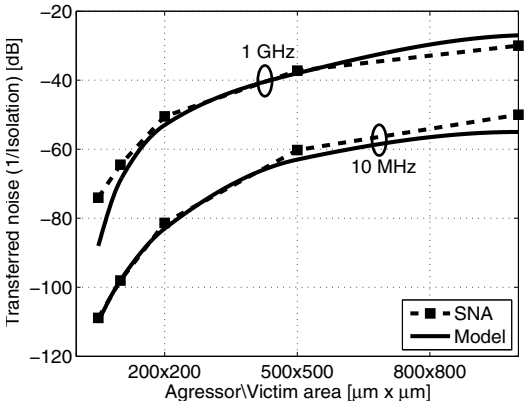

Fig. 6. Magnitude of transferred noise as a function of circuit size for a triple well with a guard ring structure.

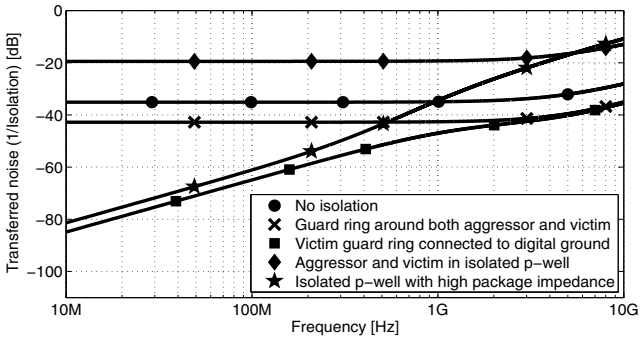

Fig. 7. Comparison of the isolation efficiency of several different configurations obtained using the proposed models.

lightly doped substrate: (1) no isolation, (2) both aggressor and victim are surrounded with guard rings with dedicated ground pads, (3) the guard ring of the victim is connected to the digital ground pad, (4) both aggressor and victim are placed in an isolated p-well with low package impedances, and (5) both aggressor and victim are placed in an isolated p-well with high package impedances. Note that the physical area of each case is maintained equal for a fair comparison. The results are illustrated in Fig. 7. An important observation is that the isolation obtained in the third case is worse than no isolation since the switching noise of the digital circuit directly couples to the victim. A guard ring should therefore have a dedicated ground pad to be effective. Another interesting observation is the effect of the package impedance on the efficiency of a triple well. Specifically, if the package impedance is sufficiently high, the first case (no isolation) achieves a better result at higher frequencies than a triple well. This result is due to a greater junction capacitance since the size of the local n-well is larger when a deep n-well is used, as shown in Fig 5. Also note that a triple well is significantly more effective than a guard ring at lower frequencies due to capacitive isolation, but the difference in efficiency diminishes as the frequency increases.

IV. Conclusions

A compact model is proposed to efficiently estimate the substrate resistances within a lightly doped substrate by approximating the current flow with a half-ellipse. Only one fitting parameter is required as opposed to existing models that use multiple fitting parameters. The proposed model is used to develop circuit descriptions of common signal isolation structures such as a guard ring and triple well. The efficiency of these isolation structures is accurately evaluated using the proposed models. These results can be used to improve overall signal integrity of mixed-signal circuits.

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