Methodology for Efficient Substrate Noise Analysis in Large-Scale Mixed-Signal Circuits

Emre Salman, *Student Member, IEEE*, Renatas Jakushokas, *Student Member, IEEE*, Eby G. Friedman, *Fellow, IEEE*, Radu M. Secareanu, *Member, IEEE*, and Olin L. Hartin

***Abstract*—A methodology is proposed to efficiently analyze substrate noise coupled to a sensitive block due to an aggressor digital block in large-scale mixed-signal circuits. The methodology is based on identifying *voltage domains* on the substrate by exploiting the small spatial voltage differences on the ground distribution network of the aggressor circuit. Specifically, similarly biased regions on the substrate short-circuited by the ground network are determined, and each of these regions is represented by a single equivalent input port to the substrate. The remaining ports within that domain are ignored to reduce the computational complexity of the extraction process. An algorithm with linear time complexity is proposed to merge those substrate contacts exhibiting a voltage difference smaller than a specified value, identifying a voltage domain. An equivalent contact is placed at the geometric mean of the merged contacts, ignoring all of the remaining ports such as the source/drain junctions of the devices. The ground network impedance is updated for each merged contact based on the proposed algorithm to maintain sufficient accuracy of the noise voltage. The substrate with reduced input ports is extracted using an existing extraction tool to analyze the noise at the sense node. As compared to the full extraction of an aggressor circuit, the methodology achieves a reduction of more than four orders of magnitude in the number of extracted substrate resistors with a peak-to-peak error of 24%.**

***Index Terms*—Ground noise, high level analysis methodology, mixed-signal ICs, substrate coupling noise, substrate extraction, substrate noise analysis.**

I. Introduction

THE continuous miniaturization of complementary metal-oxide-semiconductor (CMOS) technology enables integration of diverse functionalities on the same substrate in a system-on-chip (SoC) to achieve higher performance and reduced cost [1]–[3]. These mixed-signal systems consist of aggressive digital blocks with high switching activity factors such as a microprocessor or digital signal processor. These aggressor blocks coexist with sensitive analog/RF subcircuits such as low noise amplifiers (LNA), voltage controlled oscillators (VCO), analog filters, and high-precision analog-to-digital and digital-to-analog converters. These analog/RF blocks are highly sensitive to switching noise generated by the digital circuitry [4]. Although the power and ground distribution network of these sensitive blocks are often separate from the digital blocks, the common substrate forms a conductive path between the aggressor and sensitive blocks, degrading performance [5], [6], or causing the circuit to fail [7].

The noise couples into the substrate through three primary mechanisms [8]: 1) coupling from the source/drain junction capacitances of the transistors during switching, 2) coupling from the power and ground networks of the aggressor digital circuit, and 3) impact ionization, which is negligible as compared to the first two mechanisms, as described in [8]. The noise injected into the substrate propagates through the substrate and reaches the boundary of the sensitive circuit. The substrate noise may affect the victim block by modifying the threshold voltage of the devices through the body effect, couple into the power/ground network, or directly couple into the analog/RF signal lines.

The accurate and efficient estimation of the substrate coupling noise, and functional verification of the circuit in the presence of this noise has become an important design issue. Estimating substrate coupling noise in a large-scale circuit such as a transceiver, however, is a challenging task since the circuit activity, power/ground network, and the substrate network should be simultaneously considered, significantly increasing the computational complexity of the estimation process. A high level analysis methodology to reduce the computational complexity while achieving reasonable accuracy is, therefore, required.

A methodology is introduced in this paper to efficiently analyze the substrate noise generated by an aggressor digital block. The methodology is based on identifying voltage domains within the substrate of the aggressor circuit. A voltage domain represents a region within the substrate that is biased with approximately the same voltage by substrate contacts, and is, therefore, shorted by the ground network. These voltage domains are determined from the differences in the transient voltage among the substrate contacts, where each domain is represented by a single equivalent contact, thereby reducing the overall number of input ports for extraction. For n number of input ports, a minimum of $(n^2 - n)/2$ number of substrate resistors are required to model the substrate if a quasi-static approximation is assumed. A reduction in the number of input ports, therefore, quadratically reduces the number of extracted substrate resistors.

A linear time algorithm is proposed to determine the voltage domains within a substrate by analyzing the transient voltage differences among the substrate contacts. Those contacts exhibiting a voltage difference smaller than a specified value are

Manuscript received November 20, 2007; revised April 07, 2008. First published March 16, 2009; current version published September 23, 2009. This work was supported in part by the Semiconductor Research Corporation under Contract 2004-TJ-1207, in part by the National Science Foundation under Contract CCF-0541206, in part by grants from the New York State Office of Science, Technology and Academic Research to the Center for Advanced Technology in Electronic Imaging Systems, and in part by grants from Intel Corporation, Eastman Kodak Company, and Freescale Semiconductor Corporation.

E. Salman, R. Jakushokas, and E. G. Friedman are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: salman@ece.rochester.edu; jakushok@ece.rochester.edu; friedman@ece.rochester.edu).

R. M. Secareanu and O. L. Hartin are with Freescale Semiconductor, Microwave and Mixed-Signal Technologies, Tempe, AZ 85284 USA (e-mail: r54143@freescale.com; lee.hartin@freescale.com).

Digital Object Identifier 10.1109/TVLSI.2008.2003518

merged, and an equivalent contact is placed at the geometric mean of the merged contacts. The impedance of the ground network is updated to maintain accuracy. This methodology achieves more than four orders of magnitude reduction in the number of substrate resistors as compared to the full extraction of the circuit at the expense of 24% error in the peak-to-peak substrate noise voltage.

The rest of the paper is organized as follows. Existing high level substrate noise analysis methodologies and substrate modeling techniques are summarized in Section II. The proposed methodology is described in Section III. The simulation results of two different circuits are provided in Section IV. Finally, the paper is concluded in Section V, followed by a discussion of future work and limitations of the methodology in Section VI.

II. Problem Formulation and Background

Existing approaches for high level substrate noise analysis are summarized in Section II-A. Existing substrate modeling techniques and associated limitations are reviewed in Section II-B. The process of identifying *voltage domains* across the substrate in order to reduce the computational complexity of the extraction process is introduced in Section II-C.

A. Existing High Level Substrate Noise Analysis Approaches

A schematic based analysis methodology has been proposed in [9] to reduce the number of elements obtained from the post-layout extraction process. The transistor level simulation of a large-scale circuit including the back annotation of the substrate resistance of every port, however, is not feasible for large-scale circuits due to the nonlinear nature of the device models.

A methodology is proposed in [10] for accurately estimating the switching current drawn by a digital block. Two different techniques are introduced: an input pattern dependent scheme for high accuracy and a pattern independent scheme for high computational efficiency. Current profiles are used to analyze the substrate noise. Efficient modeling of the substrate network of a large-scale circuit, however, remains as the primary issue.

A high-level simulation methodology is provided in [11] by generating a macro model for each standard cell in the circuit. The proposed approach is, however, challenging, particularly for bulk type substrates where the substrate cannot be represented by a single equipotential node. Shorting all of the substrate contacts to a single node, as suggested in [11], is not a valid approach for those packaging techniques where the pad inductance is relatively low (such as a flip-chip package), and, therefore, the on-chip inductance becomes important. Furthermore, various blocks exist in a complex SoC exhibiting different switching activities, thereby causing on-chip ground bounce variations within the circuit. The methodology proposed in this paper considers these on-chip ground bounce variations, and determines those substrate contacts shorted by the ground network to improve computational efficiency.

B. Existing Substrate Modeling Approaches

Current approaches to model the substrate can be divided into two classes. The first class includes those techniques that discretize the substrate into a 3-D $R(C)$ mesh to determine the impedances such as the finite difference method (FDM) [12], [13] and the boundary element method (BEM) [14], [15]. Neglecting magnetic field effects on the substrate, a simplified Maxwell's equation can be derived as

$$\frac{1}{\rho}\Delta \bullet E + \epsilon\frac{\partial}{\partial t}(\Delta \bullet E) = 0 \tag{1}$$

where ρ and ϵ represent, respectively, the sheet resistivity and the permittivity of the semiconductor, and E is the electric field.

Equation (1) can discretize the substrate volume in *differential* form using FDM, resulting in a huge, sparse matrix. Although the nonuniformities distributed throughout the substrate can be included using FDM [16], the overall accuracy is a strong function of the resolution of the discretization process, making the extraction of bulk-type substrates challenging [7].

Alternatively, (1) can be discretized in *integral* form using BEM with an appropriate Green's Function [17]. For BEM, the size of the resulting matrix is significantly smaller, yet highly dense, as compared to FDM, since BEM only discretizes the ports into the substrate. As such, BEM does not consider the nonuniformity of the substrate such as channel stop implants.

Several different techniques have been proposed to obtain a more efficient solution of the algebraic equations produced by FDM or BEM to reduce an *RC* network such as moment matching techniques [18], [19], a fast Fourier transform algorithm [15], a fast eigendecomposition technique [16], a numerically stable Green Function [20], and a combination of BEM and FEM techniques [21]. The primary limitation of these approaches (FDM and BEM), however, is the increase in computational complexity with the size of the circuit, prohibiting the efficient analysis of large-scale mixed-signal circuits.

The second class of substrate modeling methods is the use of macromodels to represent the impedance between two ports on a substrate [22], [23]. Although computationally more efficient as compared to FDM and BEM, only limited accuracy can be achieved. Other limitations of these macromodels are the requirement to use process-dependent fitting parameters obtained through empirical data and scaling these models for smaller geometries.

A methodology is proposed in this paper to improve the computational complexity of the substrate extraction process by reducing the number of input ports of the aggressor circuit. The number of input ports is reduced *before* initiating the extraction process by exploiting the small spatial voltage differences within the ground network of the aggressor circuit, as described in Section II-C.

C. Voltage Domains on the Substrate

In a mixed-signal circuit, a common approach to bias the substrate of a digital block is to connect the substrate to the digital ground network with substrate contacts. Due to the parasitic impedance of the ground network, each substrate contact has an $IR + L\,\partial i/\partial t$ voltage bounce which resistively couples into the substrate. As such, if the voltage variation between a set of substrate contacts is sufficiently small, the corresponding area of the substrate is effectively short-circuited by these contacts, as illustrated in Fig. 1.

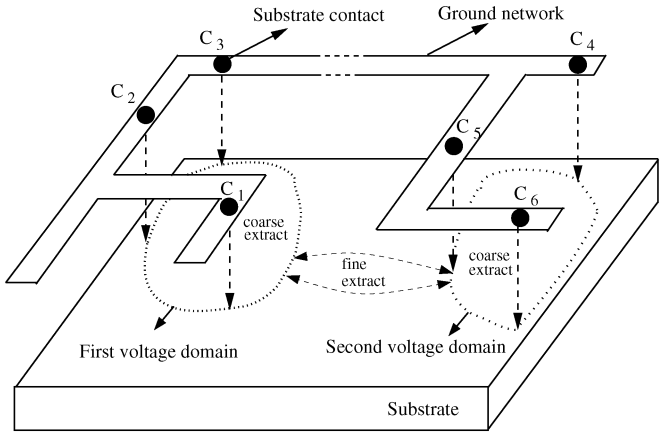


Fig. 1. Identifying the voltage domains within the substrate. Assuming $V_{C1} \approx V_{C2} \approx V_{C3}$ and $V_{C4} \approx V_{C5} \approx V_{C6}$, two voltage domains are created by the first and last three contacts. A coarse extraction is performed within each domain to reduce the computational complexity, followed by a fine extraction of those domains where the dominant current flow occurs.

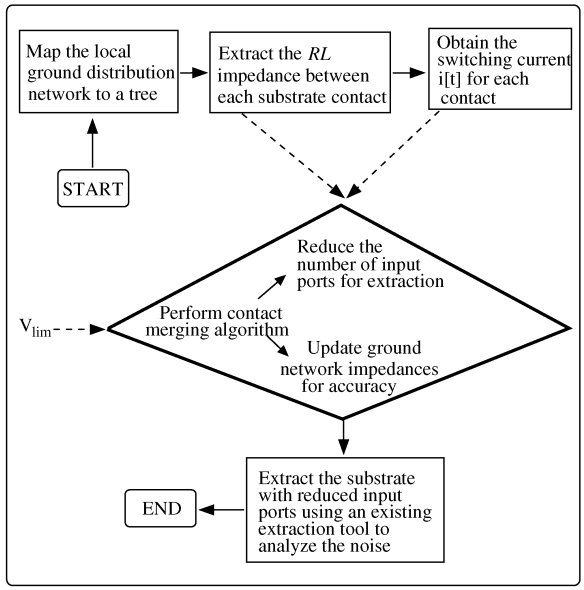


Fig. 2. Flowchart summarizing the proposed methodology to analyze substrate noise in a large-scale mixed-signal circuit.

The transient voltage difference between two contacts C_1 and C_2 is determined by

$$V_{C1} - V_{C2} = V_{12} = i(t)_{12} R_{12} + L_{12} \frac{\partial i(t)_{12}}{\partial t} \qquad (2)$$

where $i(t)_{12}$ is the transient current of the ground network flowing from C_1 to C_2 injected by the switching gates. R_{12} and L_{12} are, respectively, the parasitic resistance and inductance of the ground network between C_1 and C_2. Referring to Fig. 1, the transient voltage difference among the contacts C_1, C_2, and C_3 and among C_4, C_5, and C_6 is assumed to be sufficiently small such that, respectively, $V_{C1} \approx V_{C2} \approx V_{C3}$ and $V_{C4} \approx V_{C5} \approx V_{C6}$. As a result, the corresponding area biased by the first three contacts determines the first voltage domain on the substrate and, similarly, the last three contacts determine the second voltage domain. Since the voltage variations within a domain are sufficiently small, the dominant current flow occurs *among* these voltage domains. The small spatial voltage differences within the ground network can, therefore, be exploited to reduce the overall number of input ports for extraction.

An algorithm is described in this paper to identify these voltage domains on the substrate. An equivalent contact is created for each domain while neglecting the other ports within that domain. The number of input ports is reduced, significantly improving the computational complexity of the extraction process.

III. Substrate Noise Analysis Methodology

The proposed methodology for efficiently estimating the substrate noise generated by an aggressive digital circuit consists of five steps, as described below and also illustrated in the flowchart shown in Fig. 2.

- **Step 1**. The local ground distribution network is extracted to obtain the parasitic resistance and inductance between each substrate contact. In a digital integrated circuit, the power/ground network is designed in a hierarchical fashion, as shown in Fig. 3 [24], [25]. The upper metal layers span the entire die, forming a regular global mesh. The purpose of these upper metal layers is to distribute power/ground while minimizing the ohmic and inductive losses throughout the die. Power is supplied to the devices in each macroblock by means of the local power distribution network which can be generally represented as a tree. Note that the substrate contacts are located on the first metal layer, and therefore, are part of the local ground network. The proposed approach assumes an ideal ground for those points where the local tree is connected to the global mesh. Consequently, the local ground network can be mapped to a tree data structure where each substrate contact is a node and the ideal ground is the root of the tree.

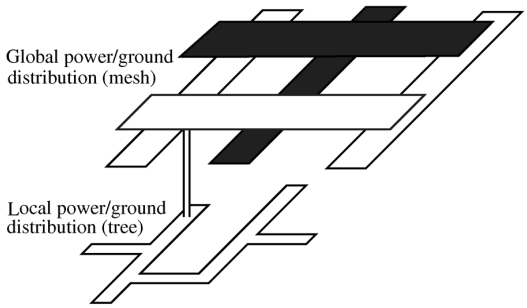


Fig. 3. In a typical power/ground distribution network, upper metal layers span the entire die, forming a global mesh. The power/ground network is distributed to the devices in each macroblock through the local distribution network, represented as a tree.

- **Step 2**. The current injected into each substrate contact by the switching circuit is characterized over a specific time window for a specific set of input vectors generating sufficient switching activity. For a large digital block, these current profiles can be obtained by precharacterizing each standard cell within each library followed by a behavioral simulation of the circuit to extract the switching time of

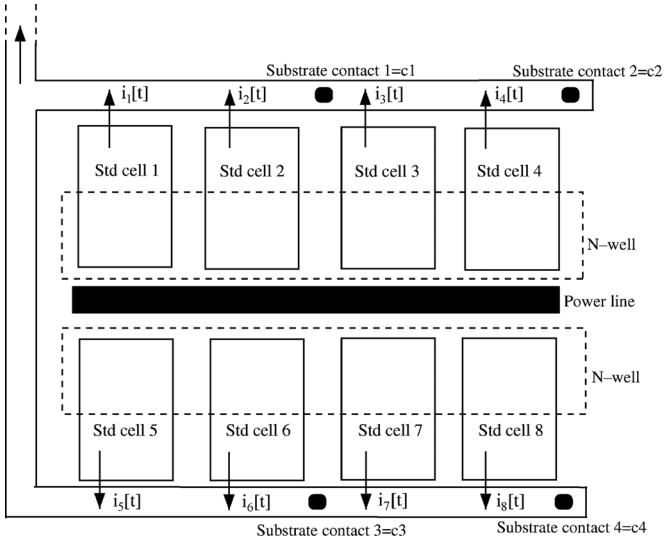


Fig. 4. Current injected into each substrate contact by the switching circuit is characterized over a specific time window. The current injected by those cells located between two contacts is shifted to the previous contact such that $i_{c1}[t] = i_1[t] + i_2[t]$, $i_{c2}[t] = i_3[t] + i_4[t]$, $i_{c3}[t] = i_5[t] + i_6[t]$, and $i_{c4}[t] = i_7[t] + i_8[t]$.

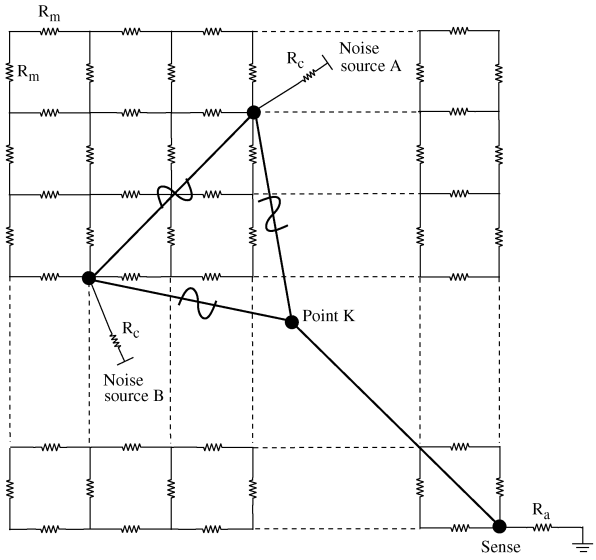


Fig. 5. Two substrate contacts A and B acting as noise sources, where the substrate is represented as a 2-D resistive mesh.

each cell [10], [26]. The current injected by those cells located between two contacts is shifted to the previous contact to prevent overly optimistic results, as illustrated in Fig. 4. The total switching current injected into the first substrate contact (c_1) is equal to $i_1[t] + i_2[t]$. Similarly, for the second substrate contact (c_2), the injected current is equal to $i_3[t] + i_4[t]$. The transient voltage difference between c_1 and c_2 is, therefore, approximated as $(i_3[t] + i_4[t])Z(12)$ where $Z(12)$ is the RL impedance between the contacts, as determined by Step 1. Note that this approximation is pessimistic since the average current flowing through this impedance is, in reality, less than $i_3[t] + i_4[t]$.

- **Step 3**. The proposed algorithm is performed to determine the voltage domains based on the data obtained from the first two steps and an additional parameter $V_{\lim}$ that defines the condition when to merge a set of contacts. The ground network impedances are updated based on the algorithm to maintain sufficient accuracy. Note that $V_{\lim}$ provides flexibility to exploit accuracy versus complexity tradeoffs, as described in Section IV.
- **Step 4**. For each voltage domain determined in Step 3, an equivalent contact with the same physical size is placed at the geometric mean of the merged contacts. All of the remaining ports into the substrate within that voltage domain, such as the source/drain regions of the devices, are neglected to reduce the computational complexity.
- **Step 5**. The substrate is extracted with these equivalent contacts which are also connected to the updated ground network. The resulting netlist is analyzed to determine the substrate noise at the sense node located around the sensitive block.

A theoretical analysis of the methodology is provided in Section III-A. The contact merging algorithm identifying the voltage domains and creating an equivalent contact for each domain is described in Section III-B. Bounds on the error in estimating the substrate noise are discussed in Section III-C. The time complexity of the contact merging algorithm is analyzed in Section III-D.

A. Theoretical Analysis

Each substrate contact behaves as a noise source, injecting ground noise into the substrate. These contacts are considered as input ports for the extraction of the substrate. In the best case, $(n^2-n)/2$ number of substrate resistances are required to model the substrate with n number of input ports. If, however, the noise on a set of input ports is sufficiently close, these ports identify a voltage domain that can be represented by an equivalent port, reducing the overall number of input ports that need to be extracted.

This reduction in the number of input ports is demonstrated by a simple example, as illustrated in Fig. 5, where the substrate is modeled as a 2-D resistive mesh. Points A and B represent two substrate contacts with noise voltages, respectively, V and $V-\varepsilon$. Note that these noise voltages are due to the switching current flowing through the parasitic impedance of the ground network. R_c represents the substrate contact resistance. K is a location on the substrate where the distance among the points A, B, and K is identical. The sense node is connected to the analog ground with a resistance R_a. This circuit is modeled with equivalent resistances, as shown in Fig. 6(a), where R_s is the equivalent substrate resistance among points A, B, and K, and R_d is the equivalent substrate resistance between point K and the sense node. Based on Fig. 6(a), the noise V_{ab}^s at the sense node due to two noise sources A and B is

$$V_{ab}^s = \frac{R_a(2V - \varepsilon)}{2R_a + 2R_d + R_s + R_c}. \tag{3}$$

Assuming the two noise sources A and B are merged into a single noise source C, as shown in Fig. 6(b), the noise V_{eqn}^s at the sense node due to this equivalent noise source is

$$V_{eqn}^s = \frac{4R_aV}{4R_a + 4R_d + 3R_s + 4R_c}. \tag{4}$$

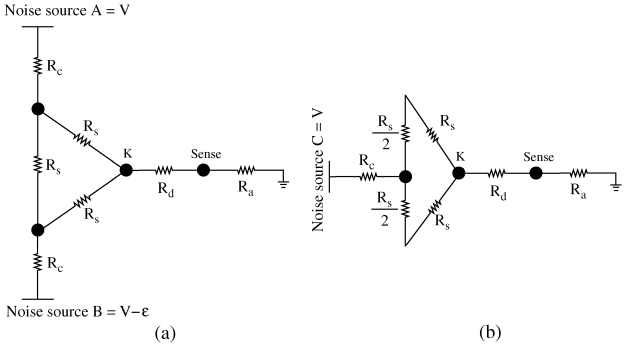


Fig. 6. Equivalent circuit to analyze the impact of two noise sources with similar noise voltages on the substrate: (a) before merging, (b) after merging.

The error in merging the two noise sources into an equivalent noise source is

$$E = \left| V_{ab}^{s} - V_{eqn}^{s} \right|. \tag{5}$$

The contact resistance R_c is typically in the range of ohms and, therefore, much smaller than the substrate resistance R_s which is in the range of kiloohms for a bulk type substrate [27]. Similarly, R_s is much smaller than R_d assuming the sense node is far from the noise sources. The error can, therefore, be approximated as

$$E \approx \frac{R_a \varepsilon}{2R_a + 2R_d}. \tag{6}$$

Since R_a is also much smaller than R_d, the error can be further simplified to

$$E \approx \frac{R_a \varepsilon}{2R_d}. \tag{7}$$

Note that ε is the voltage difference between the substrate contacts A and B that are merged into a single noise source C. This voltage difference is scaled by $R_a/2R_d$ where $R_d \gg R_a$ to determine the error at the sense node on the substrate. The error, therefore, grows with increasing ε (or V_{lim} in the proposed algorithm) and decreases with increasing physical distance between the noise sources and the sense node.

As an example, the substrate is modeled as a 25 × 25 mesh where the unit resistance R_m and the substrate contact resistance R_c are determined, respectively, as 3 KΩ and 18 Ω for a 90 nm CMOS technology with $V_{dd} = 1.2$ V with a bulk type substrate. Assuming the ground bounce is within 15% of V_{dd}, two substrate contacts with noise voltages, respectively, 80 mV and 100 mV, are placed on the substrate as illustrated in Fig. 5. The resistance R_a is extracted as 1.4 KΩ using SubstrateStorm assuming the sense node is placed within a p+ guard ring with ten analog substrate contacts. The circuit is analyzed using SPICE and the noise at the sense node is determined as 12.8 mV. If these two noise sources are merged, the noise at the sense node is 13.2 mV with a single equivalent noise source. Noise sources with different noise voltages and the error at the sense node obtained from SPICE simulations and (5) are listed in Table I. Note that the equivalent resistances R_s and R_d are determined from the mesh, respectively, as 3.4 KΩ and 8.54 KΩ. The SPICE results obtained from simulating the mesh are compared with (5). Note that the error increases with increasing ε.

TABLE I
ERROR COMPARISON DUE TO MERGING CONTACTS OBTAINED BY SPICE AND (5) FOR DIFFERENT NOISE VOLTAGES

	V_a (mV)	V_b (mV)	Noise at sense (mV)	Error (mV) SPICE	Error (mV) Eqn. (5)
Before merge	80	100	12.8	0.4	0.37
After merge	100		13.2		
Before merge	80	120	14.3	1.5	1.41
After merge	120		15.8		
Before merge	80	160	17.1	3.9	3.5
After merge	160		21		

This example demonstrates that the noise sources with approximately equal voltages can be represented with a single noise source with sufficiently small error due to the mesh structure of the substrate. The proposed algorithm to reduce the overall number of input ports *before* extracting the substrate by exploiting this characteristic is described in the following section.

B. Contact Merging Algorithm

The extracted local ground network (including the substrate contacts) of the aggressor circuit is mapped to a tree data structure where each substrate contact and intersection are represented as nodes. The root of the tree is represented by the ideal ground where the local tree is connected to the global mesh. Each node in the tree is characterized by seven elements.

- $i_{[t]}(\text{node})$ represents the switching current profile *injected* into the node by the switching gates. Note that each current profile includes the switching time information which is obtained at a specific time window and stored in an array at discrete time points. This timing information is obtained through a gate level behavioral simulation of the digital circuit.
- $i_{\text{out}[t]}(\text{node})$ represents the total switching current profile flowing from the node towards the parent of the node.
- $R(\text{node})$ represents the parasitic resistance of the ground interconnect between the node and the parent of the node.
- $L(\text{node})$ represents the parasitic inductance of the ground interconnect between the node and the parent of the node.
- $C_x(\text{node})$ represents the x_{th} child of the node.
- $nc(\text{node})$ represents the number of children of the node.
- $V_{\text{diff}}(\text{node})$ represents the peak value of the transient voltage difference between the node and the parent of the node.

An example structure is shown in Fig. 7 to illustrate these elements, and the inputs and outputs of the algorithm.

The algorithm traverses the entire tree starting from the leaf nodes to evaluate the voltage difference $V_{\text{diff}}(\text{node})$ between each node and parent. If the peak value of this transient voltage difference is smaller than the limit voltage V_{lim}, which is an input parameter, those nodes are merged into a single node and the node voltage is updated by modifying the resistance and inductance to maintain the absolute voltage with the least error. Note that rather than calculating the absolute voltages to determine whether the nodes should be merged, the voltage *difference* between the nodes, based on the current profile and the parasitic impedances, is sufficient. The analysis of the voltage difference rather than the absolute voltages significantly reduces the complexity and memory requirements of the algorithm.

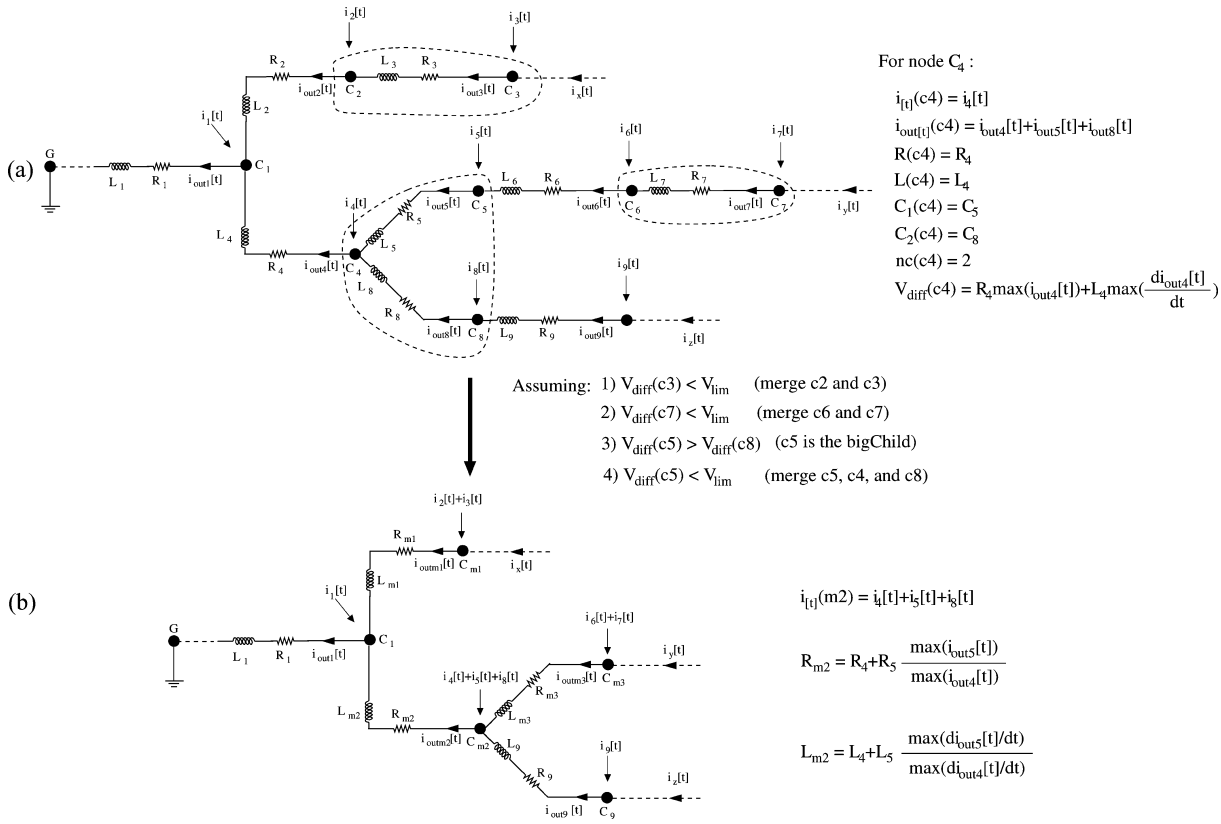


Fig. 7. First metal layer of the digital ground network mapped to a tree where each node represents a substrate contact and the root is assumed to be the ideal ground where the local tree is connected to the global mesh: (a) before merging. All seven elements are illustrated for node C_4, (b) after merging. Note that $i_{[t]}(\mathrm{node})$, $R(\mathrm{node})$, and $L(\mathrm{node})$ are updated as shown for node C_{m2} to maintain the voltage on the node with the least error.

```
MERGE-CONTACTS(node, V_lim)
1.  if node =! leaf
2.    for x = 1:1:nc(node)
3.      MERGE-CONTACTS( C_x(node), V_lim)
4.    end
5.    i_out[t](node) = i_[t](node) + i_out[t](C_1(node)) + ... + i_out[t](C_k(node))
6.    V_(diff-max) = V_diff(C_1(node))
7.    bigChild = C_1(node)
8.    for x=2:1:nc(node)
9.      if V_diff(C_x(node)) > V_(diff-max)
10.       V_(diff-max)= V_diff(C_x(node))
11.       bigChild = C_x(node)
12.     end
13.   end
14.   if V_(diff-max) < V_lim
15.     R(node) = R(node) + R(bigChild) max(|i_out[t](bigChild)|) / max(|i_out[t](node)|)
16.     L(node) = L(node) + L(bigChild) max(|∂(i_out[t](bigChild))/∂t|) / max(|∂(i_out[t](node))/∂t|)
17.     i_[t](node) = i_[t](node) + i_[t](C_1(node)) + ... + i_[t](C_k(node))
18.     Correct(node, bigChild)
19.   end
20. end
21. V_diff(node) = R(node)max(i_out[t](node)) + L(node)max(∂(i_out[t](node))/∂t)
```

Fig. 8. Pseudo-code to merge the substrate contacts on the ground network based on spatial transient voltage differences.

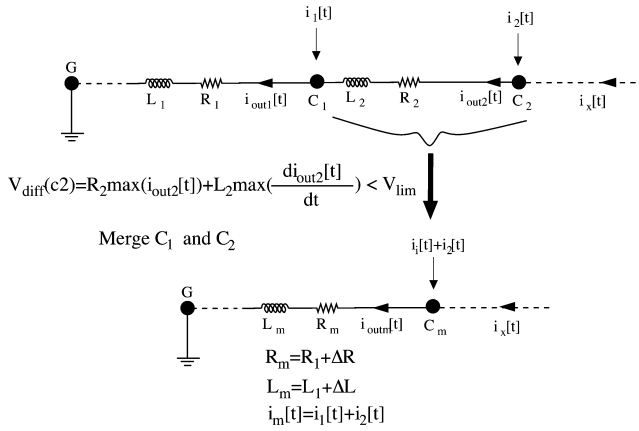


Fig. 9. Illustration of impedance updated after merging two nodes. The resistance and inductance are incremented, respectively, by ΔR and ΔL to maintain the original voltage with the least error.

Pseudo-code of the proposed recursive algorithm MERGE-CONTACTS is provided in Fig. 8. The algorithm starts with the *root* and V_{lim}, as specified by the user, for the first and second arguments, respectively. In lines 1–4, MERGE-CONTACTS is recalled for each node in the tree until the leaves are reached. The peak voltage difference $V_{\mathrm{diff}}(\mathrm{node})$ between each leaf and the parent is calculated in line 21. In lines 6–13, the child with the greatest voltage difference between the parent is identified and called *bigChild*. If this voltage difference is smaller than V_{lim}, all of the children and the parent are merged into one node and the resistance, inductance, and the switching current profile of the merged node are updated in lines 15–17 to maintain the original transient voltage with the least error. The procedure for updating the impedances is illustrated in Fig. 9 for a simpler case. Assuming the peak voltage difference between C_1 and C_2 is less than V_{lim}, these two nodes are merged into C_m. The resistance and inductance of C_m are incremented, respectively,

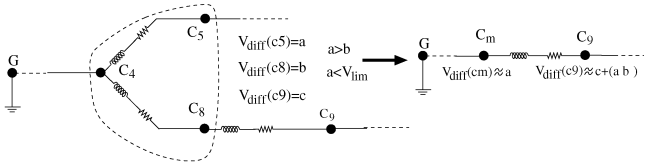


Fig. 10. Illustration of the $Correct$ function. After the nodes C_4, C_5, and C_8 are merged based on $V_{\rm diff}(c5)$, $V_{\rm diff}(c9)$ shifts by $(a-b)$ which is compensated by the $Correct$ function.

by ΔR and ΔL to compensate for the voltage loss caused by merging C_1 and C_2 such that

$$i_{\rm out2}[t]R_2 + L_2\frac{\partial i_{\rm out2}[t]}{\partial t} = \Delta R i_{{\rm out}m}[t] + \Delta L\frac{\partial i_{{\rm out}m}[t]}{\partial t}. \quad (8)$$

Since $i_{{\rm out}m}$ is equal to $i_{\rm out1}$, ΔR and ΔL are given by, respectively

$$\Delta R = R_2\frac{max\left(|i_{\rm out2}[t]|\right)}{max\left(|i_{\rm out1}[t]|\right)} \quad (9)$$

$$\Delta L = L_2\frac{max\left(|\partial i_{\rm out2}[t]/\partial t|\right)}{max\left(|\partial i_{\rm out1}[t]/\partial t|\right)}. \quad (10)$$

Note that the algorithm maintains the peak value of the absolute voltage after merging. As such, the maximum value of the currents are considered when updating the impedance. Another option is to consider the rms value rather than the maximum value. The rms value, however, produces a larger error in the substrate noise. Assuming $i_x[t] = 0$ in Fig. 9, (9) and (10) can be rewritten as

$$\Delta R = R_2\frac{max\left(|i_2[t]|\right)}{max\left(|i_1[t] + i_2[t]|\right)} \quad (11)$$

$$\Delta L = L_2\frac{max\left(|\partial i_2[t]/\partial t|\right)}{max\left(|\partial\left(i_1[t] + i_2[t]\right)/\partial t|\right)}. \quad (12)$$

The updated resistance and inductance of the merged node C_m are, therefore, respectively

$$R_m = R_1 + \Delta R \quad (13)$$

$$L_m = L_1 + \Delta L. \quad (14)$$

If the node has more than one child, merging and updating the impedance of the merged node is achieved based on $bigChild$. For example, in Fig. 7(a), C_4 has two children, C_5 and C_8. Assuming $V_{\rm diff}(c5)$ is greater than $V_{\rm diff}(c8)$ and less than $V_{\rm lim}$, C_5 is identified as the $bigChild$, and C_4, C_5, and C_8 are merged into one node C_{m2}. The resistance and inductance of the merged node are updated based on C_5, as shown in Fig. 7(b).

Since the nodes are merged based on the voltage difference of $bigChild$, a correction is required to maintain the original transient voltage for other children to prevent error accumulation, which is achieved by the $Correct$ function in line 18. An example of this process is shown in Fig. 10, illustrating the requirement for this function.

Assuming that $V_{\rm diff}(c5) = a$ is greater than $V_{\rm diff}(c8) = b$, and less than $V_{\rm lim}$; nodes C_4, C_5, and C_8 are merged where $bigChild$ is C_5. After merging, the impedance of the merged node C_m is adjusted to make $V_{\rm diff}(cm)$ approximately equal to a. After merging, the new parent of C_9 is C_m, and $V_{\rm diff}(c9)$ shifts by $a-b$. Note that the error for C_9 accumulates with additional merging. In order to prevent this error accumulation, the impedance of C_9 is updated by the $Correct$ function to compensate for the error $a-b$. Pseudo-code for the $Correct$ function is shown in Fig. 11. The voltage required to compensate this error is calculated in lines 2 and 3. The resistance and inductance are correspondingly updated in lines 5 and 6. The upper bounds on the error due to contact merging are discussed in the following section.

Correct(node, bigChild)
1. **for** k = 1:1:nc(node)
2. $V_{corr}(R)$ = max[$R(bigChild)\ i_{out[t]}(bigChild)$ - $R(C_k(node))\ i_{out[t]}(C_k(node))$]
3. $V_{corr}(L)$ = max[$L(bigChild)\frac{\partial i_{out[t]}(bigChild)}{\partial t}$ - $L(C_k(node))\frac{\partial i_{out[t]}(C_k(node))}{\partial t}$]
4. **for** p = 1:1:$nc(C_k(node))$
5. $R(C_p(C_k(node)))$ = $R(C_p(C_k(node)))$ - $\frac{V_{corr}(R)}{max[|i_{out[t]}(C_p(C_k(node)))|]}$
6. $L(C_p(C_k(node)))$ = $L(C_p(C_k(node)))$ - $\frac{V_{corr}(L)}{max[|\frac{\partial i_{out[t]}(C_p(C_k(node)))}{\partial t}|]}$
7. **end**
8. **end**

Fig. 11. Pseudo-code of the $Correct$ function to prevent error accumulation after merging a set of contacts.

C. Bounds on Error

As described in the previous section, the decision as to which contacts to merge is achieved based on the transient voltage difference among the contacts over a specific time window. The maximum voltage difference over this time window is compared with $V_{\rm lim}$ to determine whether the contacts can be merged. The resistance and inductance of a merged contact are updated, respectively, in (13) and (14) to maintain the peak value of the absolute voltage on the ground network. Referring to Fig. 9, the error $E[t]$ on the ground network due to merging contacts C_1 and C_2 into an equivalent contact C_m is determined by

$$E[t] = |V_{c2}[t] - V_{cm}[t]| \quad (15)$$

where V_{c2} and V_{cm} are the voltages across, respectively, C_2 and C_m. For a single merge operation, the upper bound for this error is $2 \times V_{\rm lim}$ (see the Appendix). For n number of merges resulting in n number of voltage domains, the error is bounded by $2n \times V_{\rm lim}$, assuming the error introduced by each merge accumulates. In practice, however, the error does not reach this value since the error values accumulate only if the maximum error of each merge occurs at the same time. Furthermore, the maximum error does not occur at the peak voltage since the algorithm maintains the peak value of the voltage after merging. An example of the maximum error for each contact is illustrated in Fig. 12 for two arbitrary ground networks. In Fig. 12(a), the ground network is composed of a single line with 60 substrate contacts. $V_{\rm lim}$ is equal to 50 mV, generating six voltage domains, as illustrated in Fig. 12(a). The peak error for each contact is below the upper bound. Note that the error is sufficiently small at the beginning of a voltage domain and gradually increases to $V_{\rm lim}$ as additional contacts are merged, as illustrated by the diagonal arrow in Fig. 12(a). When the maximum number of contacts to be merged is reached, the error exhibits a sudden decrease and starts to rise again for the following voltage domain. In Fig. 12(b), the error of each contact is depicted for a tree

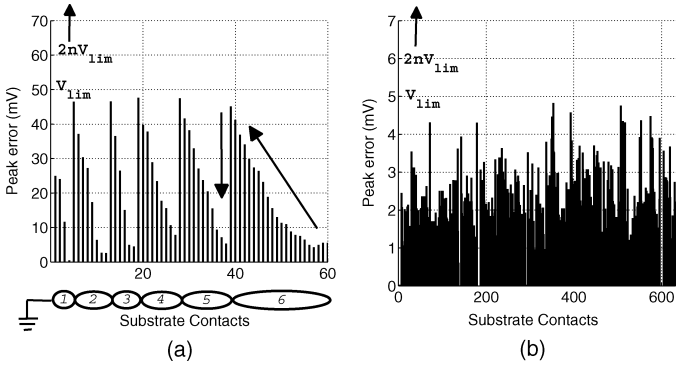


Fig. 12. Maximum error in the voltage of each contact due to merging: (a) ground network is composed of a single line with 60 substrate contacts, $V_{\rm lim} = 50$ mV. Six voltage domains are identified. (b) Ground network is composed of a tree with 632 substrate contacts, $V_{\rm lim} = 5$ mV. 105 voltage domains are identified.

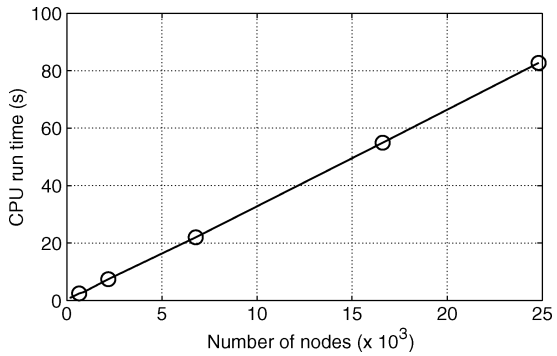


Fig. 13. Dependency of CPU run time on the number of nodes, demonstrating the linear complexity of the algorithm.

structured ground network consisting of 632 substrate contacts where $V_{\rm lim} = 5$ mV. Note that the voltage error at the substrate contact determined from (15) and illustrated in Fig. 12 is scaled by the substrate resistance between the contact and the sense node to determine the error in the substrate noise at the sense node, as described in Section III-A.

D. Complexity Analysis

In order to evaluate the time complexity of MERGE-CONTACTS, the total number of substrate contacts is N, where each contact is represented as a node in a tree. In the worst case, for N number of nodes in a tree, $N-1$ merges can be achieved. For each merge, lines 5–17 shown in Fig. 8 require a time proportional to the number of discrete time points in the current waveforms t. Line 18 requires time proportional to $k \times l$, where k is the number of children of the node and l is the number of grandchildren. The time complexity of MERGE-CONTACTS is, therefore, $O(N \times (kl+t))$, which reduces to linear time complexity $O(N)$ since k, l, and t are constants. The algorithm, as implemented in Matlab, has been performed for various number of nodes. The dependence of the CPU run time on the number of nodes is illustrated in Fig. 13, demonstrating the linear complexity of the algorithm.

IV. Simulation Results

The proposed CONTACT-MERGE algorithm has been implemented in Matlab to evaluate the proposed methodology.

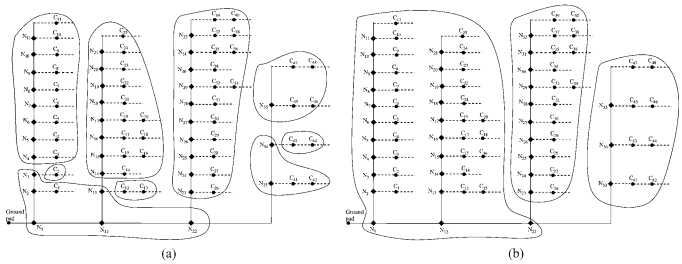


Fig. 14. Voltage domains on the substrate as determined by the CONTACT-MERGE algorithm: (a) $V_{\rm lim} = 0.1$ V. Nine voltage domains are identified. (b) $V_{\rm lim} = 0.25$ V. Three voltage domains are identified.

Two different aggressor circuits have been analyzed to quantify the computational complexity and accuracy of the methodology. The results obtained from the first and second circuits are described, respectively, in Sections IV-A and IV-B. The proper selection of $V_{\rm lim}$ for the algorithm is discussed in Section IV-C.

A. Circuit 1

The first circuit consists of a 4-bit carry select adder, a control unit, and scaled buffers at the output, designed in a 0.18 μm CMOS technology on a bulk type substrate. The parasitic resistance of the ground network is determined from the sheet and via resistances. The sheet resistances are 95 mΩ and 80 mΩ for the first and second metal layer, respectively, and the via resistance is 2 Ω. Note that the parasitic inductance of the ground network is neglected for this first circuit. The switching current waveform $(i_{[t]}(\text{node}))$ for each contact is obtained through a transistor level simulation for a specific time window since this circuit has been designed in a full custom design methodology.

The CONTACT-MERGE algorithm is performed to identify the voltage domains on the substrate. Four different voltages (0.05 volts, 0.1 volts, 0.25 volts, and 0.4 volts) are used for $V_{\rm lim}$ to investigate the complexity versus accuracy tradeoff. For $V_{\rm lim} = 0.1$ V, nine voltage domains are identified. If $V_{\rm lim}$ is increased to 0.25 volts, three voltage domains are determined. Each of these domains is represented by an equivalent substrate contact placed at the geometric mean of the merged contacts. These domains are illustrated in Fig. 14. The dashed lines represent the first metal layer and the solid lines represent the second metal layer of the ground network. The substrate contacts are represented by circles. The diamonds represent the intersection of two metal lines in the ground network. Note that the switching current for these nodes represented by a diamond is zero since these nodes do not represent substrate contacts.

As shown in Fig. 14(a), a fewer number of nodes are merged for those contacts closer to the ground pad. This behavior is due to the large voltage difference among these contacts since the overall switching current flowing among these contacts is relatively high. Similarly, depending upon the switching activity, a fewer number of substrate contacts are merged for those blocks that inject higher current. Contacts C_{41} to C_{48}, shown in Fig. 14(a), belong to those output buffers sinking higher current as compared to the other blocks in the circuit. Three different voltage domains are, therefore, determined for these substrate contacts.

The substrate is extracted for the pre- and postmerging cases using SubstrateStorm [28]. The noise is observed using Spectre

TABLE II
ORIGINAL AND UPDATED $R(\text{node})$ VALUES OF C_{41} TO C_{48} FOR DIFFERENT VALUES OF V_{lim}

	$R(node)$ (Ω)			
	Original	$V_{lim} = 0.05$ volts	$V_{lim} = 0.1$ volts	$V_{lim} = 0.25$ volts
C_{41}	4.3	8.2	16.7	19
C_{42}	4			
N_{33}	10.9	10.9		
N_{34}	7	14	3.1	
C_{43}	4.3			
C_{44}	4			
N_{35}	7		15.8	
C_{45}	4.3	8.2		
C_{46}	4			
C_{47}	11.3	15		
C_{48}	4			

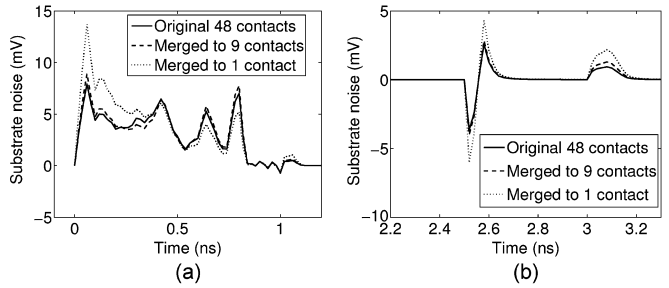


Fig. 15. Comparison of the substrate noise at the sense node before and after merging for two different time intervals: (a) from 0 to 1.2 ns, (b) from 2.2 ns to 3.2 ns. The solid line represents the original circuit with 48 substrate contacts. The dashed and dotted lines represent, respectively, the reduced network with nine substrate contacts ($V_{\text{lim}} = 0.1$ V) and a single substrate contact ($V_{\text{lim}} = 0.4$ V). The peak-to-peak error in the noise voltage is 11% for nine substrate contacts and increases to 70% for a single substrate contact. The error in the rms noise voltage over one period is 6% for nine contacts and increases to 28% for a single contact.

at the sense node located 60 μm from the nearest substrate contact. Note that the parasitic resistance among the substrate contacts on the ground network ($R(\text{node})$) and the current profile of each contact ($i_{[t]}(\text{node})$) are updated after merging based on the CONTACT-MERGE algorithm, as described in Section III-B. As an example, the value of the original and updated $R(\text{node})$ after merging is listed in Table II for C_{41} to C_{48}. For example, for $V_{\text{lim}} = 0.1$ V, C_{45} to C_{48} are merged into one node, and the updated resistance of this node is determined as 15.8 Ω. Similarly, for $V_{\text{lim}} = 0.05$ V, C_{41} and C_{42} are merged into one node with an updated resistance of 8.2 Ω.

The time domain noise waveforms observed at the sense node before and after merging are compared in Fig. 15 at two different time intervals. The waveform shape and peak magnitude of the substrate noise at the sense node after merging into nine contacts match the original noise voltage with a peak-to-peak error of 11% in the noise voltage. Note that the error increases to 70% if V_{lim} is increased to 0.4 volts, merging all of the contacts into a single contact. The error in the rms noise over one period is 6% for nine contacts and increases to 28% for a single contact.

The frequency domain characteristics are illustrated in Fig. 16. The ratio of the estimated power of the noise to the original power is less than 1 dB at the fundamental frequency (200 MHz), and four higher harmonics when $V_{\text{lim}} = 0.1$ V (the number of contacts is reduced to nine). For $V_{\text{lim}} = 0.4$ V (where the number of contacts is reduced to one), this ratio

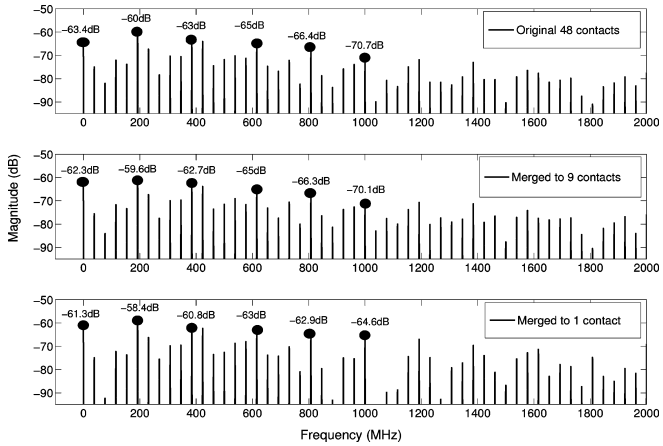


Fig. 16. Comparison of the spectrum of the substrate noise at the sense node before and after merging into nine contacts ($V_{\text{lim}} = 0.1$ V) and a single contact ($V_{\text{lim}} = 0.4$ V).

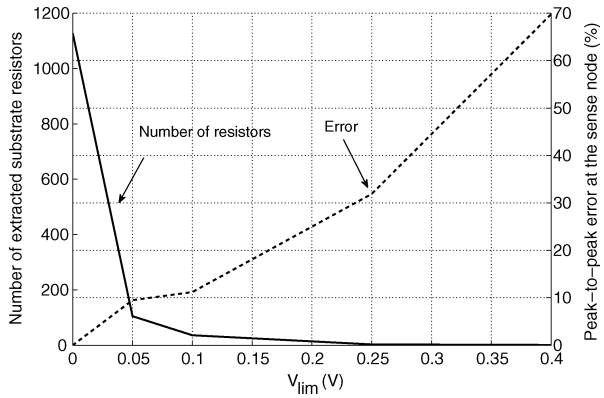


Fig. 17. Number of extracted substrate resistors and the error in the peak-to-peak noise voltage at the sense node as a function of V_{lim} for circuit 1. The solid and dashed curves represent, respectively, the number of resistors and the error.

increases to 1.6 dB at the fundamental frequency. Note that in this case the ratio further increases at the higher harmonics, for example, 6 dB at 1 GHz.

Considering the number of substrate resistances, SubstrateStorm extracts 1128 resistors in the original system with 48 substrate contacts. Alternatively, when the number of contacts is reduced to nine, the number of extracted substrate resistances is 36, corresponding to a 31X reduction in extracted resistors. The dependence of the error and number of extracted substrate resistors on V_{lim} is shown in Fig. 17 to illustrate the complexity versus accuracy tradeoff.

Note that a rapid reduction in the number of resistors is achieved with a relatively small V_{lim}. Increasing V_{lim} above 0.1 volts marginally improves the complexity while introducing additional error at the sense node. These results are listed in Table III for four different values of V_{lim}.

B. Circuit 2

The second circuit is an aggressor digital core located close to a sensitive block in an industrial transceiver circuit, designed in a 90 nm CMOS technology on a bulk type substrate. The circuit contains approximately 200 standard cells. This second circuit is used for two purposes: to examine the behavior of the algorithm

TABLE III
REDUCTION IN THE NUMBER OF EXTRACTED SUBSTRATE RESISTORS, SUBSTRATE NOISE AT THE SENSE NODE, AND THE CORRESPONDING ERROR IN THE SUBSTRATE NOISE FOR DIFFERENT VALUES OF $V_{\rm lim}$ IN CIRCUIT 1

	Number of substrate contacts	Number of extracted substrate resistors	Reduction	Noise at the sense node: Peak-to-peak (mV)	RMS (mV)	At 200 MHz (dB)	Error at the sense node: Peak-to-peak (%)	RMS (%)	Estimated / Original At 200 MHz (dB)
Original	48	1128	–	11.6	0.68	-60	–	–	–
$V_{lim} = 0.05$ V	15	105	11x	10.5	0.61	-60.9	9.5	10.3	-0.9
$V_{lim} = 0.1$ V	9	36	31x	12.9	0.72	-59.6	11.2	5.9	0.4
$V_{lim} = 0.25$ V	3	3	376x	15.3	0.78	-58.9	31.9	14.7	1.1
$V_{lim} = 0.4$ V	1	1	1128x	19.7	0.87	-58.4	69.8	27.9	1.6

TABLE IV
ORIGINAL AND UPDATED $R(\mathrm{node})$ AND $L(\mathrm{node})$ VALUES OF C_{43} TO C_{49} FOR VARIOUS VALUES OF $V_{\rm lim}$

	$R(node)$ (Ω)				$L(node)$ (pH)			
	Original	$V_{lim} = 3$ mV	$V_{lim} = 5$ mV	$V_{lim} = 10$ mV	Original	$V_{lim} = 3$ mV	$V_{lim} = 5$ mV	$V_{lim} = 10$ mV
C_{43}	5.4	5.7	10.3	19.2	11.9	12.6	22.9	45
C_{44}	0.3				0.7			
C_{45}	4.6	6			10.3	13.4		
C_{46}	1.4		8.9		3.1		22.2	
C_{47}	3.7	7.5			8.2	19.2		
C_{48}	1.6				3.5			
C_{49}	3.8				8.3			

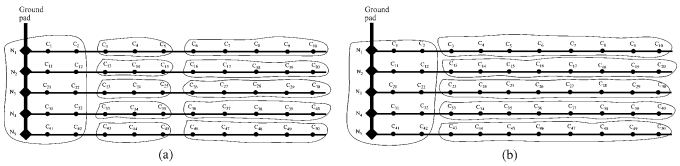


Fig. 18. Voltage domains on the substrate as determined by the CONTACT-MERGE algorithm: (a) $V_{\rm lim} = 5$ mV. Eleven voltage domains are identified. (b) $V_{\rm lim} = 10$ mV. Six voltage domains are identified.

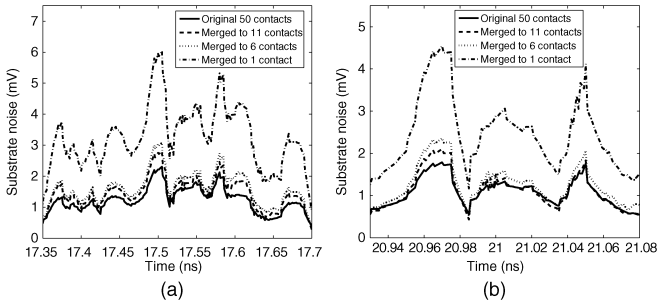


Fig. 19. Comparison of the substrate noise at the sense node before and after merging for two different time intervals: (a) from 17.35 ns to 17.70 ns, (b) from 20.93 ns to 21.08 ns. The solid line represents the original circuit with 50 substrate contacts. The dashed, dotted, and dash-dotted lines represent, respectively, the reduced network with eleven substrate contacts ($V_{\rm lim} = 5$ mV), six substrate contacts ($V_{\rm lim} = 10$ mV), and a single substrate contact ($V_{\rm lim} = 20$ mV). The peak-to-peak error in the noise voltage is 22% for eleven substrate contacts, 34% for six contacts, and increases to 160% for a single substrate contact.

for a standard cell based circuit and to evaluate the effect of the parasitic inductance of the ground network on the accuracy of the methodology.

The parasitic resistance between the nodes on the ground network is determined from the sheet resistance (72 mΩ) of the metal lines. The parasitic inductance is extracted using Q3D Extractor [29]. For the vertical ground line with a 1 μm width, the parasitic inductance is 0.79 pH/μm. For the horizontal lines with a width of 0.14 μm, the inductance is extracted as 1.14 pH/μm. The switching current waveform for each contact $(i_{[t]}(\mathrm{node}))$ is determined by characterizing each individual gate in the library for various combinations of input patterns. The timing information and input switching pattern of each gate are extracted from a behavioral simulation of the circuit.

The CONTACT-MERGE algorithm is performed with five different values of $V_{\rm lim}$: 3, 5, 10, 15, and 20 mV. Eleven and six voltage domains are determined, respectively, for $V_{\rm lim} = 5$ mV and $V_{\rm lim} = 10$ mV. These voltage domains are illustrated in Fig. 18, where the simplified ground network is obtained from the physical layout of the circuit. Note that since this block is standard cell based, the contacts are placed at regular locations to align the contacts in each row. Also note that the density of the substrate contacts is relatively high as compared to regular digital blocks due to the presence of a nearby sensitive circuit.

The substrate is extracted for the pre- and postmerging cases with SubstrateStorm. The parasitic resistance $R(\mathrm{node})$ and inductance $L(\mathrm{node})$ of each merged contact on the ground network are updated. These updated values are listed in Table IV for contacts C_{43} to C_{49}.

The substrate noise is observed at a sense node located 20 μm from the digital circuit on the side of the sensitive analog block. The time domain noise waveforms observed at the sense node before and after merging are compared in Fig. 19 for two different time intervals.

The peak-to-peak error in the substrate noise voltage is 22% for eleven substrate contacts, 34% for six contacts, and increases abruptly to 160% for a single substrate contact. The error in the rms noise over a 10 ns timing window is 7% for eleven contacts, 21% for six contacts, and increases to 134% for a single contact.

The frequency domain characteristics are illustrated in Fig. 20. At the fundamental frequency (1 GHz), the ratio of the estimated power of the noise to the original power is 3.5 dB when $V_{\rm lim} = 5$ mV (the number of contacts is reduced to eleven). For $V_{\rm lim} = 20$ mV (where the number of contacts is reduced to one), this ratio increases to 10 dB. Note that the

TABLE V
REDUCTION IN THE NUMBER OF EXTRACTED SUBSTRATE RESISTORS, SUBSTRATE NOISE AT THE SENSE NODE, AND THE CORRESPONDING ERROR IN THE SUBSTRATE NOISE FOR DIFFERENT VALUES OF $V_{\rm lim}$ IN CIRCUIT 2

	Number of substrate contacts	Number of extracted substrate resistors	Reduction	Noise at the sense node			Error at the sense node		Estimated / Original
				Peak-to-peak (mV)	RMS (mV)	At 1 GHz (dB)	Peak-to-peak (%)	RMS (%)	At 1 GHz (dB)
Original	50	1225	–	2.31	0.7	-70	–	–	–
$V_{lim} = 3$ mV	17	136	9x	2.81	0.63	-67.5	21.6	10	2.5
$V_{lim} = 5$ mV	11	55	22x	2.82	0.75	-66.5	22.1	7.1	3.5
$V_{lim} = 10$ mV	6	15	82x	3.1	0.85	-65.5	34.2	21.4	4.5
$V_{lim} = 15$ mV	3	3	408x	5.61	1.78	-59	142.8	154.3	11
$V_{lim} = 20$ mV	1	1	1225x	6	1.64	-60	159.7	134.3	10

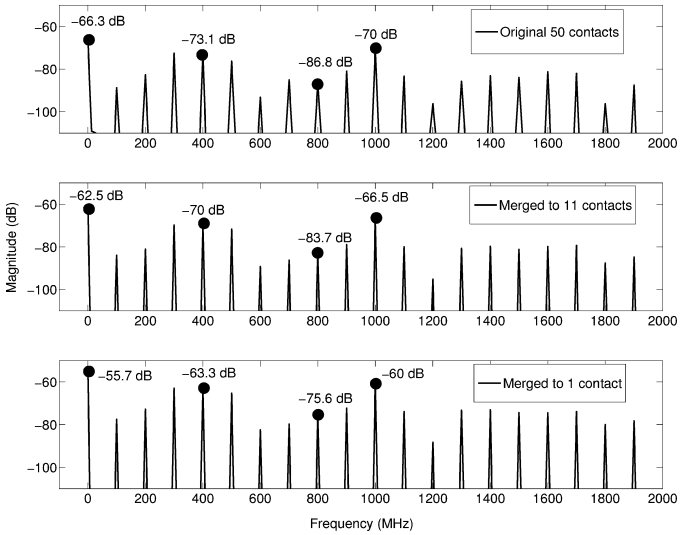


Fig. 20. Comparison of the spectrum of the substrate noise at the sense node before and after merging into eleven contacts ($V_{\rm lim} = 5$ mV) and a single contact ($V_{\rm lim} = 20$ mV).

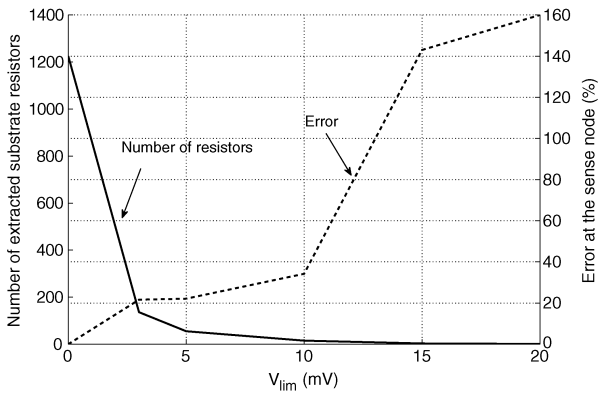


Fig. 21. Number of extracted substrate resistors and the error in the peak-to-peak noise voltage at the sense node as a function of $V_{\rm lim}$ for circuit 2. The solid and dashed curves represent, respectively, the number of resistors and the peak-to-peak error at the sense node.

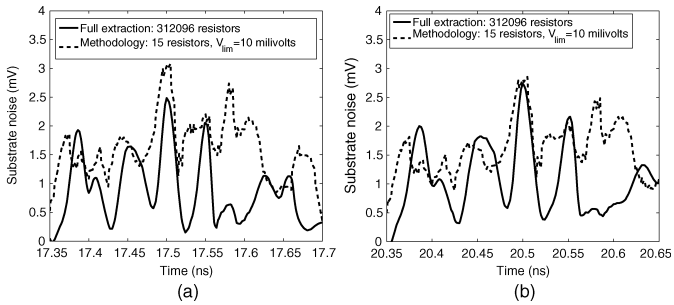


Fig. 22. Comparison of the substrate noise at the sense node obtained by simulating the fully extracted circuit and application of the methodology when $V_{\rm lim} = 10$ mV: (a) from 17.35 ns to 17.7 ns, (b) from 20.35 ns to 20.65 ns. The solid and dashed lines represent, respectively, the full extraction and methodology determined noise.

ratio remains approximately the same at the harmonics of the fundamental frequency.

Considering the number of substrate resistances, SubstrateStorm extracts 1225 resistors in the original system with 50 substrate contacts. The number of extracted substrate resistors reduces to 15 when $V_{\rm lim} = 15$ mV, corresponding to a 82X reduction. These results are listed in Table V where the error and the reduction in the number of extracted substrate resistors are summarized for various values of $V_{\rm lim}$. The tradeoff between the reduction in the number of extracted resistors and the accuracy of the substrate noise voltage is further illustrated in Fig. 21.

The complete layout of the circuit including all of the devices is extracted using Assura and SubstrateStorm to compare the results obtained by the proposed methodology with a fully extracted set of impedances. The noise waveforms at the sense node obtained by simulating the fully extracted circuit and applying the methodology when $V_{\rm lim} = 10$ mV are compared in Fig. 22 for two different time intervals.

The fully extracted circuit with 200 gates consists of 312,096 resistors for the substrate and 55,856 junction and well capacitances. The full extraction and simulation of the transient noise for this circuit on a dual core 64 bit Sun machine with Linux operating system requires approximately six hours. Alternatively, the proposed methodology reduces the number of extracted substrate resistors to 15 (for $V_{\rm lim} = 10$ mV), achieving more than four orders of magnitude reduction, and requires negligible time. The peak-to-peak error of the methodology in estimating the substrate noise voltage is 24.1%, as illustrated in Fig. 22. The limitation of the methodology in terms of run time is the requirement to precharacterize each cell in the library for various input switching patterns and to perform a gate level simulation of the circuit to extract the required timing information.

Note that the reduction achieved by the methodology is expected to increase for larger scale circuits due to the increasing number of substrate contacts. Substrate contacts are usually placed based on latch-up constraints to achieve a specific contact density [30]. A common practice is to increase the density of the contacts near those aggressor blocks that can potentially affect the sensitive circuit. An aggressor digital block may,

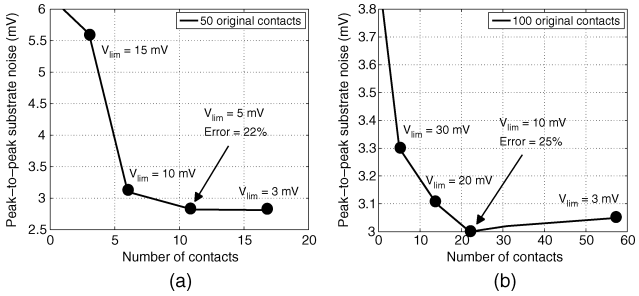


Fig. 23. Variation of the peak-to-peak noise with respect to the number of contacts after merging: (a) for the second circuit with 50 original contacts, (b) an extension of the second circuit with 100 original contacts.

therefore, require a significant number of substrate contacts, where a reduction in the number of contacts quadratically reduces the number of extracted substrate resistances. Note that this methodology achieves a reduction of more than four orders of magnitude in extracted substrate resistances as compared to a fully extracted circuit. This greater reduction is due to the increasing number of input ports in the full extraction due to the source/drain junctions of the devices which are neglected in this methodology.

C. Proper Selection of $V_{\rm lim}$

The proposed methodology requires a reasonable selection of $V_{\rm lim}$ to obtain sufficiently accurate results while reducing the overall number of extracted substrate resistors, as discussed in the previous section. Choosing a $V_{\rm lim}$ greater than the proper value significantly increases the peak-to-peak and rms error. Alternatively, an unnecessarily small $V_{\rm lim}$ limits the reduction in the extracted substrate resistors and, therefore, the computational efficiency.

A reasonable value of $V_{\rm lim}$ depends strongly on the absolute value of the peak ground bounce on the local ground distribution network of the aggressor circuit. Choosing $V_{\rm lim}$ as 20% to 30% of the peak ground bounce generally produces reasonable results. A technique is proposed in this section to properly decide the value of $V_{\rm lim}$.

As listed in Tables III and V, the peak-to-peak and rms values of the estimated noise voltage is significantly greater for the extreme case when all of the contacts are merged into one contact. As $V_{\rm lim}$ is reduced or the number of contacts is increased, the estimated noise voltages decrease, and ultimately saturate. The value where this saturation starts to occur is a good choice for $V_{\rm lim}$. The corresponding peak-to-peak noise obtained at this $V_{\rm lim}$ is reasonably accurate with respect to the fully extracted noise voltage. The variation of the peak-to-peak noise voltage with respect to the number of contacts is shown in Fig. 23 for the second circuit and an extension of the second circuit with 100 contacts.

As illustrated in Fig. 23, the peak-to-peak noise initially exhibits a rapid decrease, ultimately saturating as $V_{\rm lim}$ is decreased or the number of contacts is increased. For Fig. 23(a), at eleven contacts, the peak-to-peak error in the noise voltage is 22%. Similarly, for Fig. 23(b), the error is 25% at 22 contacts. The value of $V_{\rm lim}$ where the estimated peak-to-peak noise voltage saturates, therefore, produces sufficiently accurate results for this methodology. Note that the time complexity of the proposed algorithm is linear, allowing these iterations to be performed in a reasonable amount of time. $V_{\rm lim}$ can, therefore, be properly selected using this iterative methodology.

V. Conclusion

A methodology is proposed for the efficient analysis of substrate noise coupled to a sensitive block in large-scale mixed-signal circuits. The substrate of the aggressor circuit is partitioned into voltage domains where each domain represents a region within the substrate that is biased with approximately the same voltage by substrate contacts. Each of these voltage domains is, therefore, primarily shorted by the ground network. As such, a single equivalent input port to the substrate is generated for each domain, neglecting all of the remaining ports. The reduction in the number of input ports significantly reduces the number of extracted substrate resistors. An algorithm is proposed to determine these voltage domains by merging those contacts exhibiting a voltage difference smaller than a specified value, and generate an equivalent contact which is placed at the geometric mean of the merged contacts. The ground network impedance is updated to maintain the accuracy of the noise voltage at the sense node. Simulation results demonstrate a reduction of more than four orders of magnitude in the number of extracted substrate resistors as compared to a fully extracted layout while introducing 24% error in the peak-to-peak value of the substrate noise voltage at the sense node.

VI. Future Work and Limitations

As described in Section III, Step 2, the proposed algorithm requires current profiles for each substrate contact obtained at a specific time window. For a different window or with a different set of input vectors, these current profiles may change, affecting the merging results. This dependence of the methodology on a timing window and input vector can be improved by applying a statistical approach. Alternatively, the algorithm can be performed multiple times for different timing windows, resulting in slightly different substrate networks. This solution is computationally possible since the algorithm performs in linear time.

The proposed algorithm is independent of the location of the sensitive node where the noise is observed, assuming that the sense node is sufficiently far from the aggressor block. The dependence of the error on the specific location of the sense node is also an issue requiring additional investigation. Further reduction in the error and number of extracted resistors is possible if the location of the sense node is considered in locating the equivalent contact after merging. Also note that if the sense node is sufficiently close to the aggressor block, the physical distance among the contacts is comparable to the distance between a contact and the sense node. In this case, the location of the equivalent contact plays a significant role in the accuracy of the algorithm. Determining the specific location of the equivalent contact relative to the location of the sense node is also a focus of future study.

The current version of the algorithm assumes that the local ground distribution network of the aggressor block can be represented as a tree. This assumption may not always be valid if the aggressor block has multiple connections to the global ground network, creating a mesh. The extension of this methodology to a mesh structure is another focus of future study. One practical

approach is to assume that every connection to the upper metal layers is an additional ideal pad, and to partition the gates such that each pad sinks the current of a subclass of the gates, as proposed in [31] for placing decoupling capacitors.

APPENDIX I
UPPER BOUND ON THE ERROR

Referring to Fig. 9, C_1 and C_2 are merged into C_m if

$$V_{\text{diff}}(c2) = R_2 max\left(i_2[t]\right) + L_2 max\left(\frac{\partial i_2[t]}{\partial t}\right) < V_{\text{lim}}. \quad (16)$$

Note that $i_x[t]$ is assumed to be zero to simplify the analysis. The error $E[t]$ due to this merging is determined from (15). Using (13) and (14), this error can be rewritten as

$$\begin{aligned} E[t] = \Bigg| & i_2[t]R_2 + L_2\frac{\partial i_2[t]}{\partial t} - \left(i_1[t] + i_2[t]\right) \\ & \times R_2\frac{max\left(|i_2[t]|\right)}{max\left(|i_1[t] + i_2[t]|\right)} \\ & - L_2\frac{max\left(|\partial i_2[t]/\partial t|\right)}{max\left(|\partial\left(i_1[t] + i_2[t]\right)/\partial t|\right)} \\ & \times\frac{\partial\left(i_1[t] + i_2[t]\right)}{\partial t}\Bigg|. \end{aligned} \quad (17)$$

Two cases need to be investigated to determine the upper bound for this expression: 1) the first two terms are greater than zero and the last two terms are smaller than zero, and 2) the first two terms are smaller than zero and the last two terms are greater than zero. Assuming the first case holds, the error is

$$\begin{aligned} E[t] = & i_2[t]R_2 + L_2\frac{\partial i_2[t]}{\partial t} + \left(i_1[t] + i_2[t]\right) \\ & \times R_2\frac{max\left(|i_2[t]|\right)}{max\left(|i_1[t] + i_2[t]|\right)} \\ & + L_2\frac{max\left(|\partial i_2[t]/\partial t|\right)}{max\left(|\partial\left(i_1[t] + i_2[t]\right)/\partial t|\right)} \\ & \times\frac{\partial\left(i_1[t] + i_2[t]\right)}{\partial t} \end{aligned} \quad (18)$$

where each term is greater than zero. Since

$$\frac{\left(i_1[t] + i_2[t]\right)}{max\left(|i_1[t] + i_2[t]|\right)} \leq 1 \quad (19)$$

and

$$\frac{\partial\left(i_1[t] + i_2[t]\right)/\partial t}{max\left(|\partial\left(i_1[t] + i_2[t]\right)/\partial t\right)} \leq 1 \quad (20)$$

the error expression is

$$\begin{aligned} E[t] \leq i_2[t]R_2 + L_2\frac{\partial i_2[t]}{\partial t} + R_2 max\left(|i_2[t]|\right) \\ + L_2 max\left(|\partial\left(i_2[t]\right)/\partial t|\right). \end{aligned} \quad (21)$$

The summation of the first two terms and the last two terms on the right side of the inequality is smaller than V_{lim}, as determined by (16). The upper bound of the error due to merging C_1 and C_2 into a single contact is, therefore, $2 \times V_{\text{lim}}$

$$E[t] \leq 2V_{\text{lim}}. \quad (22)$$

Note that the same bound holds for the second case where the first two terms in (17) are smaller than zero and the last two terms are greater than zero.

REFERENCES

[1] T. Kadoyama *et al.*, "A complete single-chip GPS receiver with 1.6-V 24-mW radio in 0.18- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 562–568, Apr. 2004.

[2] A. Koukab, K. Banerjee, and M. Declercq, "Analysis and optimization of substrate noise coupling in single-chip RF transceiver design," in *Proc. IEEE/ACM International Conf. Computer-Aided Design*, Nov. 2002, pp. 309–316.

[3] S. Kiaei, D. Allstot, K. Hansen, and N. K. Verghese, "Noise considerations for mixed-signal RF IC transceivers," *ACM J. Wireless Netw.*, vol. 4, pp. 41–53, Jan. 1998.

[4] B. Badaroglu *et al.*, "Modeling of substrate noise generation, isolation, and impact for an LC-VCO and a digital modem on a lightly-doped substrate," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2040–2051, Sep. 2006.

[5] C. Soens *et al.*, "Performance degradation of LC-tank VCOs by impact of digital switching noise in lightly doped substrates," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1472–1481, Jul. 2005.

[6] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits," *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 420–430, Apr. 1993.

[7] N. K. Verghese, D. J. Allstot, and M. A. Wolfe, "Verification techniques for substrate coupling and their application to mixed-signal IC design," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 354–365, Mar. 1996.

[8] J. Briaire and K. S. Krisch, "Principles of substrate crosstalk generation in CMOS circuits," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 19, no. 6, pp. 645–653, Jun. 2000.

[9] P. Birrer, S. K. Arunachalam, M. Held, K. Mayaram, and T. S. Fiez, "Schematic-driven substrate noise coupling analysis in mixed-signal IC designs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 12, pp. 2578–2587, December 2006.

[10] S. M. Reddy and R. Murgai, "Accurate substrate noise analysis based on library module characterization," presented at the IEEE Int. Conf. VLSI Design, Jan. 2006.

[11] B. Badaroglu *et al.*, "SWAN: High-level simulation methodology for digital substrate noise generation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 1, pp. 23–33, Jan. 2006.

[12] K. Fukahori and P. R. Gray, "Computer simulation of integrated circuits in the presence of electrothermal interaction," *IEEE J. Solid-State Circuits*, vol. 11, no. 6, pp. 834–846, Dec. 1976.

[13] B. R. Stanisic, N. K. Verghese, R. A. Rutenbar, R. Carley, and D. J. Allstot, "Addressing substrate coupling in mixed-mode IC's: Simulation and power distribution synthesis," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 226–238, Mar. 1994.

[14] T. Smedes, N. P. van der Meijs, and A. J. van Genderen, "Boundary element methods for 3D capacitance and substrate resistance calculations in inhomogeneous media in a VLSI layout verification package," *Adv. Eng. Softw.*, vol. 20, no. 1, pp. 19–27, 1994.

[15] R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 344–352, Mar. 1996.

[16] J. P. Costa, M. Chou, and L. M. Silveria, "Efficient techniques for accurate modeling and simulation of substrate coupling in mixed-signal IC's," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 18, no. 5, pp. 597–607, May 1999.

[17] T. Smedes, N. P. van der Meijs, and A. J. van Genderen, "Extraction of circuit models for substrate crosstalk," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, Nov. 1995, pp. 199–206.

[18] N. K. Verghese, D. J. Allstot, and S. Masui, "Rapid simulation of substrate coupling effects in mixed-mode ICs," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1993, pp. 18.3.1–18.3.4.

[19] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 9, no. 4, pp. 352–366, Apr. 1990.

[20] A. M. Niknejad, R. Gharpurey, and R. G. Meyer, "Numerically stable green function for modeling and analysis of substrate coupling in integrated circuits," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 17, no. 4, pp. 305–315, Apr. 1998.

[21] E. Schrik and N. P. van der Meijs, "Combined BEM/FEM substrate resistance modeling," in *Proc. IEEE/ACM Des. Autom. Conf.*, Jun. 2002, pp. 771–776.
[22] D. Ozis, T. Fiez, and K. Mayaram, "A comprehensive geometry-dependent macromodel for substrate noise coupling in heavily doped CMOS processes," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2002, pp. 497–500.
[23] H. Lan *et al.*, "Synthesized compact models and experimental verifications for substrate noise coupling in mixed-signal ICs," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1817–1829, Aug. 2006.
[24] M. Popovich, A. V. Mezhiba, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors*. New York: Springer Verlag, 2008.
[25] M. Zhao, R. V. Panda, S. S. Sapatnekar, and D. Blaauw, "Hierarchical analysis of power distribution networks," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 21, no. 2, pp. 159–168, Feb. 2002.
[26] E. Charbon, P. Miliozzi, L. P. Carloni, A. Ferrari, and A. Sangiovanni-Vincentelli, "Modeling digital substrate noise injection in mixed-signal IC's," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 18, no. 3, pp. 301–310, Mar. 1999.
[27] S. Donnay and G. Gielen, *Substrate Noise Coupling in Mixed-Signal ASICs*. New York: Springer, 2003.
[28] Assura RCX, SubstrateStorm, Spectre Tools [Online]. Available: http://www.cadence.com
[29] Q3D Extractor Tool [Online]. Available: http://www.ansoft.com
[30] R. R. Troutman, *Latch-up in CMOS Technology: The Problem and Its Cure*. New York: Springer, 1986.
[31] S. Zhao, K. Roy, and C. Koh, "Decoupling capacitance allocation and its application to power-supply noise-aware floorplanning," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 21, no. 1, pp. 81–92, Jan. 2002.

Emre Salman (S'02) received the B.S. degree in microelectronics engineering from Sabanci University, Istanbul, Turkey, in 2004, and the M.S. degree in electrical and computer engineering from the University of Rochester, Rochester, NY, in 2006, where he is currently pursuing the Ph.D. degree in electrical engineering.

He was a co-op student at STMicroelectronics, Istanbul, between October 2003 and May 2004, where he worked on the design and verification of a clock and data recovery circuit for a multichannel fiber-optic transceiver. In summer 2005, he interned at Synopsys, Inc., Mountain View, CA, where he worked on pessimism reduction in static timing analysis (STA) and cell library characterization. During the summers of 2006 and 2007, he was with Freescale Semiconductor Corporation, Tempe, AZ, where he worked on circuit and physical level signal isolation methodologies with application to monolithic transceivers in CMOS and BiCMOS technologies. His research interests include analysis, modeling, and design methodologies for high-performance digital and mixed-signal integrated circuits, focusing on switching noise and timing characteristics, signal and power integrity, and the design of on-chip global interconnects such as power and clock networks.

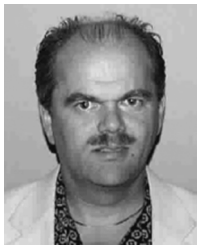
Renatas Jakushokas (S'09) received the B.Sc. degree in electrical engineering from Ort-Braude College, Karmiel, Israel, in 2005, and the M.S. degree in electrical and computer engineering from the University of Rochester, Rochester, NY, in 2007. He is currently pursuing the Ph.D. degree in electrical and computer engineering at the University of Rochester.

He was previously an intern at Intrinsix Corporation, Fairport, NY, in 2006, working on Sigma Delta ADCs, Eastman Kodak Company, Rochester, in 2007, working on high-performance comparators and Freescale Semiconductor Corporation, Tempe, AZ, in 2008, where he worked on evaluating substrate isolation techniques. His research interests are in the areas of power, noise, signal integrity, and optimization techniques in high performance integrated circuit design methodologies.

Eby G. Friedman (S'78–M'79–SM'90–F'00) received the B.S. degree from Lafayette College in 1979 and the M.S. and Ph.D. degrees from the University of California, Irvine, in 1981 and 1989, respectively, all in electrical engineering.

From 1979 to 1991, he was with Hughes Aircraft Company, rising to the position of manager of the Signal Processing Design and Test Department, responsible for the design and test of high performance digital and analog ICs. He has been with the Department of Electrical and Computer Engineering at the University of Rochester since 1991, where he is a Distinguished Professor. He is also a Visiting Professor at the Technion—Israel Institute of Technology, Haifa. His current research and teaching interests are in high performance synchronous digital and mixed-signal microelectronic design and analysis with application to high speed portable processors and low-power wireless communications. He is the author of more than 350 papers and book chapters, several patents, and the author or editor of ten books in the fields of high speed and low power CMOS design techniques, high speed interconnect, and the theory and application of synchronous clock and power distribution networks.

Dr. Friedman is the Regional Editor of the *Journal of Circuits, Systems and Computers*, Chair of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS steering committee, and a member of several editorial boards and conference technical program committees. He previously was the Editor-in-Chief of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, a member of the editorial board of the *Proceedings of the IEEE*, a member of the *Circuits and Systems (CAS) Society* Board of Governors, Program and Technical chair of several IEEE conferences, and a recipient of the Howard Hughes Masters and Doctoral Fellowships, the University of Rochester Graduate Teaching Award, a College of Engineering Teaching Excellence Award, and several other awards. He is a Senior Fulbright Fellow.



Radu M. Secareanu (S'96–M'00) received the Ph.D. degree from the University of Rochester, Rochester, NY, in 2000.

He worked for five years as a design R&D Engineer. Since 2000, he has been with the Microwave and Mixed-Signal Technologies Laboratory, Freescale Semiconductor (formerly Motorola SPS), Tempe, AZ. Since 2002, he has also been an Adjunct Professor with the Electrical Engineering Department, Arizona State University, Tempe. His research interests include signal integrity (substrate, interconnect, power-ground network), the relationship with new technologies and mixed-signal and RF circuit design aspects, and low-voltage and low-power circuit design. He has authored and coauthored over 30 referred papers, five issued patents, and six pending patents.

Dr. Secareanu has served in several conference committees, presented several conference tutorials, served as an IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS Associate Editor, and is actively involved in Semiconductor Research Corporation (SRC) activities. Mr. Radu is a recipient of one of the 2007 Mahboob Khan Outstanding Mentor Awards.

Olin L. Hartin was born in Seminole, TX. He attended Texas A&M University, College Station, and received the Ph.D. degree form the University of Texas.

He has lead the Device Physics and Simulation Group at Motorola and at Freescale for the last eight years. His technical contributions have been mainly in small and large signal RF device and circuit design.