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On-Chip Regulators for Low-Voltage and Portable Systems-on-Chip

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3.1 Introduction

Efficient voltage regulation and conversion are essential mechanisms in modern integrated circuit (IC) design process due to power management and heterogeneous computing [1]. Specifically, fully monolithic on-chip voltage regulation has emerged as a critical process for a variety of low-power design

methodologies, such as voltage islands (ranging from ultralow voltages in the range of 0.4–0.5 V to higher voltages in the range of 1.2–1.4 V), dynamic voltage (and frequency) scaling, low-voltage clocking, and near-threshold computing [2–4]. Furthermore, on-chip voltage regulators play a critical role to ensure sufficient power integrity since it is highly challenging to maintain power supply noise within a tolerable range when the supply voltage is low and the load current is high [5–7]. Power supply noise not only affects the timing characteristics within synchronous digital circuits, but also degrades the overall signal integrity in analog and mixed-signal circuits [8]. For example, a fully integrated voltage regulator (FIVR) was developed for the Intel Haswell microarchitecture, allowing dynamically managed multiple power domains [9].

The rest of the chapter is organized as follows. Opportunities provided by monolithic voltage regulation and related challenges are summarized in the following subsections. A broad overview of primary voltage regulator topologies is provided in Section 3.2 with emphasis on low-dropout (LDO) regulators, switched-capacitor-based regulators, and switching buck regulators. A fully monolithic hybrid regulator topology is described in Section 3.3 with application to low-voltage systems such as near-threshold computing. Finally, the chapter is summarized in Section 3.4.

3.1.1 Opportunities Provided by Monolithic Regulators

On-chip integration of a voltage regulator on the same die as the load circuit, as illustrated in Figure 3.1(b), has several advantages compared with an off-chip voltage regulator, as illustrated in Figure 3.1(a). These advantages include

- Reduction in conduction loss due to reduced parasitic interconnect impedances
- Superior voltage regulation characteristics
- Enhanced power supply noise characteristics
- Reduced number of power pads and less metal resources for multi-voltage systems

In off-chip regulators, the parasitic impedances of the interconnect among the devices, pads, and package dissipate significant energy, thereby reducing the overall efficiency of a regulator. Integrating a voltage regulator with the load circuit can potentially reduce these parasitic losses since the interconnect length is significantly shorter [10, 11].

Furthermore, a monolithic regulator outperforms an off-chip regulator in terms of regulation characteristics since the regulator is physically closer to the load, producing a faster response. Thus, the regulator exhibits reduced sensitivity to changes in the load current. The power supply noise caused by the parasitic interconnect impedances and package inductance is also reduced.

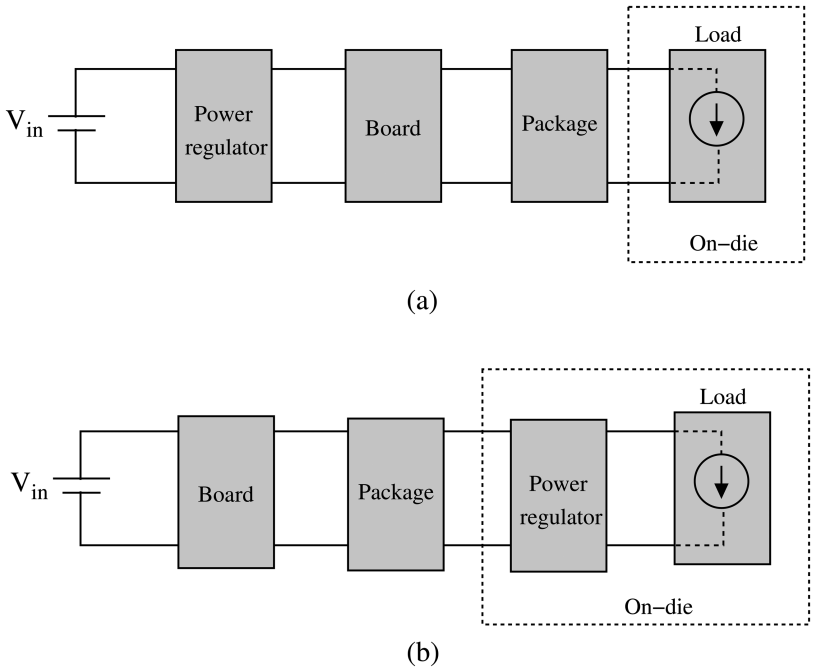

FIGURE 3.1
Conceptual representation of an (a) off-chip and an (b) on-chip power converter.

Another advantage of on-chip regulators for multivoltage systems (voltage islands) is the reduction in the number of power pads. The metal resources allocated for the global power grids are also reduced since a separate global power distribution network for each voltage is not required. Similarly, on-chip regulators are considered to be an enabling technology for dynamic voltage frequency scaling (DVFS), where the power supply voltage is temporarily adjusted based on the required computation [2,12]. This technique requires fast voltage transients, on the scale of nanoseconds, which is possible with the use of on-chip power regulators. The timing diagram of a fine-grain DVFS scheme is illustrated in Figure 3.2, where four different voltage and frequency levels are achieved using on-chip conversion [13].

3.1.2 Challenges in Designing Monolithic Regulators

Traditional trade-offs in regulator design are exacerbated when all the components are required to be on-chip. Specifically, it is highly challenging to simultaneously satisfy the following design objectives:

- Sufficiently high energy efficiency (in the range of 80%–90%) to minimize power loss during regulation and conversion, while providing the required output current

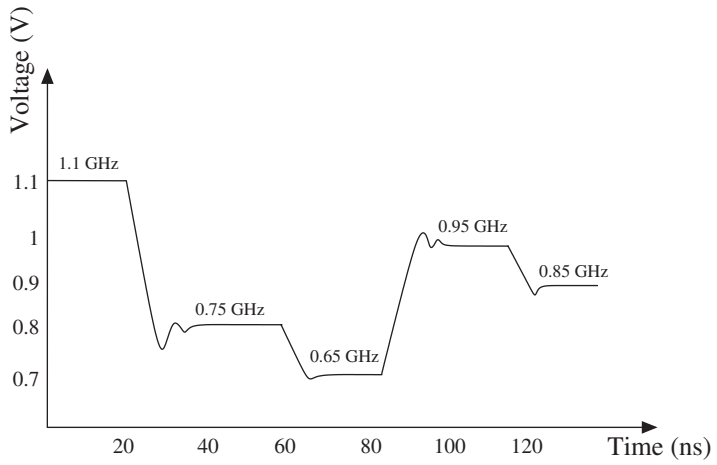

FIGURE 3.2
DVFS scheme utilizing on-chip power converters to achieve fast switching transients in the range of nanoseconds [13].

- Reasonably low physical area to reduce overall cost of the monolithic integration
- Enhanced regulation characteristics to ensure sufficiently low output voltage ripple during voltage conversion
- Sufficient thermal integrity since on-chip regulators that provide high output current are likely to cause thermal hot spots, thereby increasing the cooling cost

Linear regulators typically satisfy the area requirement and offer a low-cost solution, but fail to achieve the energy efficiency constraint. Alternatively, switching buck regulators achieve high energy efficiency due to ideally lossless circuit elements, i.e., the capacitor and inductor. Switching regulators, however, consume significant area due to these passive elements within the LC filter, particularly the inductor. Switched-capacitor-based regulators have received significant attention to simultaneously achieve the aforementioned four design objectives. An important challenge for switched-capacitor-based regulators is the difficulty of adjusting output voltage according to application requirement, i.e., achieving variable voltage conversion ratios. The primary characteristics of existing voltage regulators are described in the following section.

3.2 Overview of Primary Voltage Regulator Topologies

There are primarily three types of voltage regulators: (1) linear converters such as LDO regulators, (2) switched-capacitor-based DC-DC regulators,

and (3) switching buck regulators. These topologies are discussed in the following subsections. A qualitative comparison of these topologies is also provided in the last subsection.

3.2.1 Low-Dropout Regulators

LDO voltage regulators are a type of linear DC-DC converter where the power efficiency is enhanced by lowering the voltage drop across the pass transistor, i.e., between the input and output of the regulator. This improvement is achieved by replacing the *common drain* structure with a *common source* topology [14–17]. The voltage drop $V_{drop-out}$ is

$$V_{drop-out} = I_{in} \times R_{on}, \tag{3.1}$$

where R_{on} is the on-channel resistance of the power transistor. The power dissipation is reduced due to the smaller voltage drop, making LDO voltage regulators a suitable candidate for low-voltage, low-power applications. LDO regulators can also be used for isolating input power supply noise in noise-sensitive applications [18].

As depicted in Figure 3.3, a conventional LDO regulator is composed of an error amplifier, reference voltage generator, power transistor with a common source configuration, passive resistors to achieve voltage division, and output capacitance (or decoupling capacitance) to satisfy stability constraints. Resistors R_1 and R_2 are added since the output voltage of an LDO converter is at the drain rather than the source terminal of the

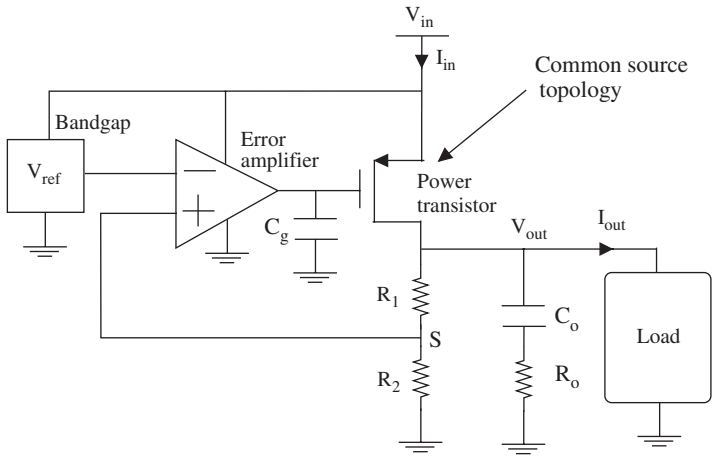

FIGURE 3.3
Block diagram of an LDO voltage regulator consisting of an error amplifier, reference voltage generator, power transistor with a common source configuration, passive resistors, and output capacitance.

power transistor. Any variation in the output voltage is sensed at node S and compared with V_{ref} by the error amplifier. The current flowing through the pass transistor is accordingly adjusted to maintain a constant output voltage. Ideally, the output voltage is maintained at $(V_{ref}/R_2) \times (R_1 + R_2)$. The temperature coefficient of the regulator is determined by the temperature dependence of the reference voltage generator and the input offset voltage of the error amplifier [18].

The design process of an LDO regulator exhibits several challenging tradeoffs. For example, the *quiescent current* of the regulator plays an important role in determining the overall power efficiency. The quiescent current refers to the input current of the regulator when there is no output (load and decoupling) capacitance. The effect of the quiescent current on the current efficiency becomes significant particularly when the load current is lower. Alternatively, for those applications where the output load current is significantly high the majority of the time, the energy efficiency is primarily determined by the ratio of the output voltage to the input voltage. In this case, LDO regulators are particularly advantageous when the voltage difference between the input and output is small. Smaller area and fast load regulation due to the small output impedance are also important advantages. However, since a higher load current is typically a temporary condition, the quiescent current has a vital effect on the overall power efficiency. Resistances R_1 and R_2 are adjusted to maintain a sufficiently low quiescent current, such as 1% of the load current [19]. A low quiescent current, however, typically degrades the transient response of the regulator, negatively affecting the regulation characteristics. The transient response time can be improved by increasing the slew rate at the output of the amplifier, which can be achieved by downsizing the power transistors. The lower bound of the size of this transistor, however, depends on the maximum current load. Finally, LDO regulators typically require a relatively large capacitor to ensure stable behavior, particularly when the open-loop gain is high. High loop gain enhances the regulation characteristics by decreasing the sensitivity of the output voltage to changes in the output current.

3.2.2 Switched-Capacitor-Based Regulators

Switched-capacitor-based regulators, also referred to as charge pump converters, utilize capacitors and several switches to achieve voltage conversion [20]. Unlike linear regulators, switched-capacitor converters can produce an output voltage that is higher or lower than the input voltage. The operating principle of a switched-capacitor DC-DC converter is illustrated in Figure 3.4, where the schematic of a *voltage doubler* is shown, without any regulation [20]. Two phase signals, ϕ_1 and ϕ_2, control the switches within the circuit. Note that these signals are out of phase to prevent any overlap. In the first phase, the phase 1 switches are closed and the phase 2 switches are open, thereby charging the capacitance C_1 to V_{in}, as depicted in Figure 3.5(a). In the

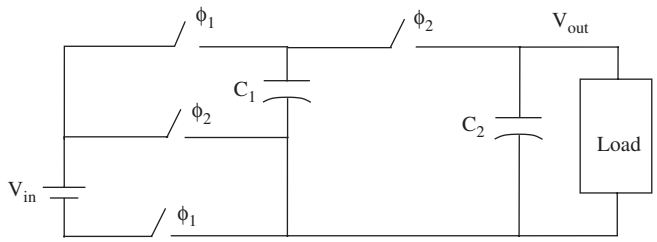

FIGURE 3.4
Schematic representation of a voltage doubler based on a switched-capacitor DC-DC converter.

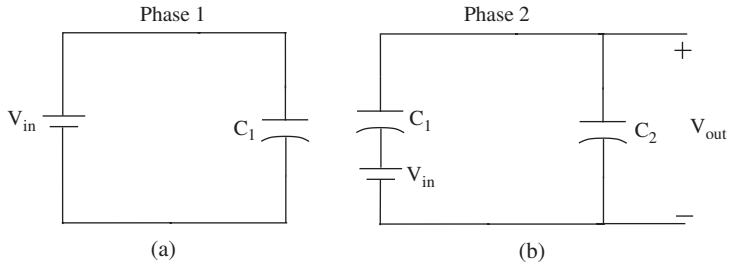

FIGURE 3.5
Operation of a switched-capacitor voltage doubler: (a) phase 1 and (b) phase 2.

second phase, as illustrated in Figure 3.5(b), the phase 2 switches are closed and the phase 1 switches are open. In this case, the input power supply voltage is connected in series with the capacitance C_1, which had been charged to V_{in} in the previous phase. This series connection produces a voltage of $2 \times V_{in}$ across the capacitance C_2, which is the output voltage applied across the load circuit. Note that the capacitance C_1 behaves as a charge pump during the second phase. Also note that during ϕ_1, the output voltage is maintained close to $2 \times V_{in}$, assuming that the switching frequency is sufficiently high. The minimum switching frequency is primarily determined by the load current characteristics and the size of C_1 and C_2. For example, the size of C_1 can be reduced if a higher switching frequency is used [21]. This dependence produces two trade-offs in the design of a switched-capacitor DC-DC converter:

- The switches are typically implemented using metal-oxide semiconductor (MOS) transistors, which are sized based on the switching frequency. The higher the switching frequency, the greater the width of these transistors. A trade-off therefore exists between the size of the capacitors and the width of the transistors operating as switches.
- As the size of the transistors increases, dynamic power dissipation also increases due to the larger gate oxide capacitance. Another

trade-off therefore exists between the switching frequency and energy efficiency of switched-capacitor DC-DC converters.

Switched-capacitor-based converters can achieve any rational conversion ratio by cascading several converters. For example, the input voltage is first multiplied by a specific integer, and divided by another integer to produce the required conversion ratio [21]. Dynamically changing this conversion ratio to adjust output voltage, however, is challenging.

As illustrated in Figure 3.4, a typical switched-capacitor DC-DC converter does not use feedback to achieve load regulation. The three methods for achieving load regulation are

- To vary C_1 to compensate for changes in the output voltage
- To vary the conductance of the switches that charge/discharge the capacitors
- To vary the duty cycle of the switching period

The first option is limited by the energy efficiency since a lower C_1 reduces the power efficiency. Alternatively, the second and third options require energy-consuming feedback circuitry, which also degrades the power efficiency.

3.2.3 Switching Buck Regulators

A switching buck regulator is a stepdown DC-DC voltage regulator to supply power to various circuit modules, such as a CPU core, memory core, or accelerator module. A typical single-phase buck converter consists of (1) a switch network that generates an AC signal, (2) a second-order low-pass filter that passes the DC component of the AC signal to the output, and (3) a feedback path that regulates the output voltage by changing the duty cycle of the AC signal [1]. These primary elements of a buck regulator are shown in Figure 3.6 where the power transistors, cascaded powers, and a pulse width modulator to regulate the output voltage are depicted. Single- and multiphase operations of a switching buck regulator are described in the following subsection.

3.2.3.1 Single-Phase Operation

Typical design specifications of a switching buck converter include input and output voltages, power efficiency, load current, voltage ripple, and transient response. The low-pass filter, consisting of an inductor and capacitor, is a critical element within the buck converter since the output voltage characteristics depend on the quality of this filter. The parasitic effective series resistance (ESR) of the inductor plays an important role in the resistive loss and the overall performance of the buck converter. A larger inductance (required

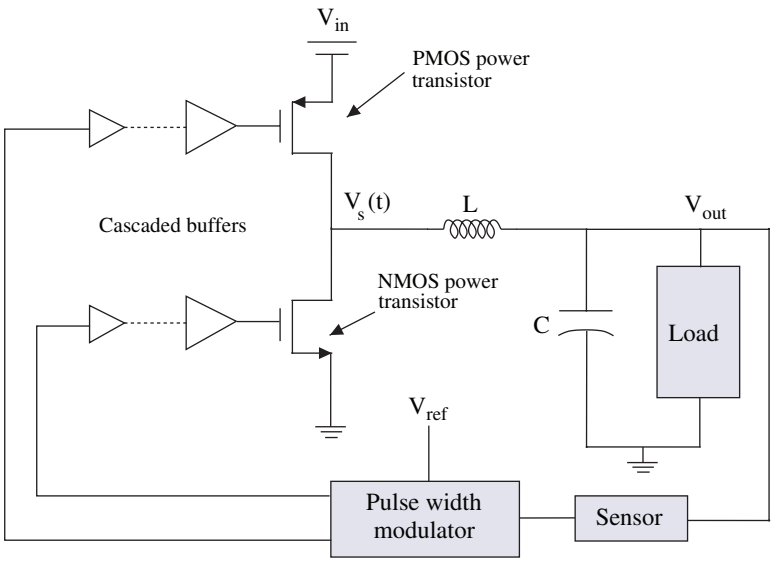

FIGURE 3.6
Schematic of a buck converter utilizing power transistors, cascaded buffers, and a pulse width modulator to regulate the output voltage.

to reduce ripple) typically produces a larger ESR, which in turn increases the resistive loss and causes a nonnegligible voltage drop at the output, particularly if the load current is sufficiently high.

For a single-phase buck converter, the required inductance can be determined by [1]

$$L = \frac{(V_{in} - V_{out})D}{2\Delta I_L f_s}, \tag{3.2}$$

where V_{in} and V_{out} are, respectively, input and output voltages, D is duty cycle, ΔI_L is the current ripple (half of the peak-to-peak current), and f_s is switching frequency. Assuming the output voltage ripple cannot exceed 5% of the output voltage, the minimum required capacitor C_{out} is determined by [1]

$$C_{out} \geq \frac{5(V_{in} - V_{out})D}{4V_{out}Lf_s^2}. \tag{3.3}$$

Single-phase buck converters are sufficient for applications with low load current [22], but power dissipation and efficiency suffer at higher load currents. Thus, interleaved multiphase buck regulators have been considered for applications with high load current since peak ripple currents can be effectively reduced through this method [23, 24]. Interleaved multiphase buck regulators are discussed in the following subsection.

3.2.3.2 Interleaved Multiphase Operation

An interleaved multiphase architecture has been commonly used to reduce the size of the individual inductors (and therefore ESR) without increasing the output ripple, as shown in Figure 3.7 [25]. In this method, since the current through each stage is reduced, the constraint on inductor current is also relaxed, thereby permitting a smaller inductor per stage. The ripple due to each stage is partially canceled at the output. Thus, a smaller output capacitance can be sufficient.

In a multiphase buck converter, the normalized ripple current I_{Rip_norm} is determined by [22]

$$I_{Rip\_norm} = P \times \frac{[D - \frac{\lfloor m \rfloor}{P}] \times [\frac{1+\lfloor m \rfloor}{P} - D]}{(1-D) \times D}, \tag{3.4}$$

where D is the duty cycle, P is the number of phases, and $m = D \times P$. This equation is important to determine the number of phases based on the required ripple current.

In this case, multiple buck converters operate in a parallel fashion with a 90° phase difference. Each regulator has an individual inductor, but shares the same output capacitor. Thus, the high ripple across each inductor is partially canceled at the output.

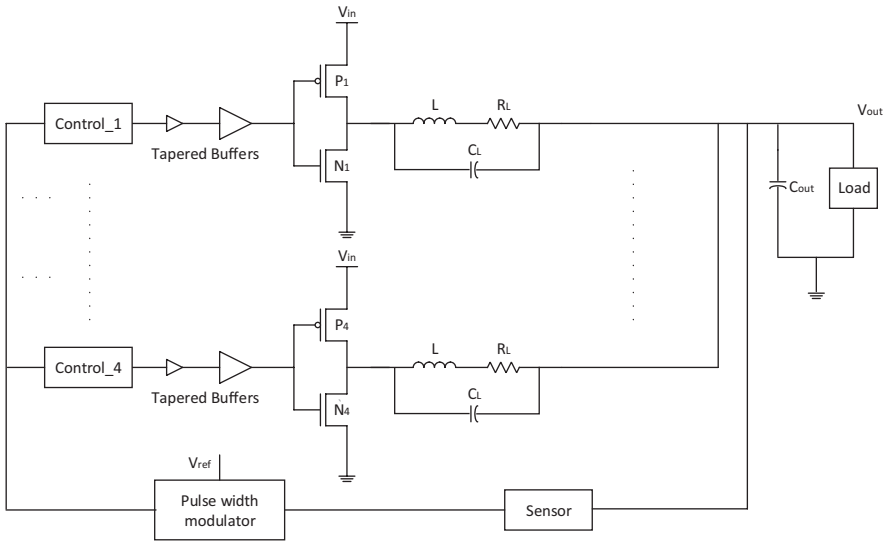

FIGURE 3.7
An interleaved multiphase switching buck regulator architecture.

3.2.4 Qualitative Comparison

LDO regulators are cost-effective and have a relatively fast transient response, but these regulators suffer from low power efficiency, less than 60% in most of the cases [26]. This limitation is exacerbated as the conversion ratio increases or output voltage decreases.

Switched-capacitor converters exhibit enhanced power efficiency at relatively small area, but suffer from poor regulation capability since the switching frequency should be modified to regulate the output [27]. This process is slow since a voltage-controlled oscillator is needed to vary the switching frequency, increasing the response time. Furthermore, it is challenging to dynamically tune the voltage conversion ratio.

Finally, switching buck converters can achieve high efficiency and large output current at the expense of a high-quality inductor [9]. Since integrating a high-quality inductor on chip is very costly, buck regulators typically consist of an external, discrete inductor. Another option is to utilize the flip-chip package for developing a package-embedded spiral inductor. For example, in [28], existing wirebond inductance of a standard package (instead of spiral metals) has been utilized for a buck converter. Similarly, in [29], both the wirebond and lead frame inductance have been engineered to be used with an integrated buck converter. These approaches reduce the overall cost (since an existing package structure is leveraged for inductance) at the expense of higher inductance variability and reduced flexibility for the value of inductance. Thus, additional mechanisms, such as extra calibration loops, are required to alleviate these challenges [28]. In [30], package-embedded inductors have been discussed with emphasis on building high-Q inductors within the routing layers of an organic package.

In [31, 32], a higher inductance with a reasonable quality factor was achieved by exploiting the greater flexibility of package area compared with die area. This package-embedded spiral inductor was connected to the die via low-resistance C4 bumps. Thus, the switching frequency of the buck regulator was reduced to minimize dynamic power loss and enhance power efficiency. Specifically, the switching frequency was 50 MHz, which is significantly smaller than typical switching frequencies used in buck regulators with on-chip inductors (477 MHz [11], 200 MHz [33], 170 MHz [34], and 300 MHz [35]). Furthermore, package flexibility can be further utilized to develop an *array of package-embedded spiral inductors* for an interleaved multiphase buck regulator architecture. Thus, power efficiency and output ripple can be further enhanced.

Existing work has also investigated the feasibility of increasing switching frequency to reduce the required inductance. In this case, however, the dynamic loss increases, thereby reducing the power efficiency [11]. For example, for inductance values in the low nanohenry range, the switching frequency should be increased to several hundreds of megahertz to obtain an acceptable current and voltage ripple at the output. The switching loss at

these frequencies increases by two orders of magnitude compared with high-kilohertz or low-megahertz operating frequencies (assuming constant transistor sizes) [29].

3.3 Monolithic Hybrid Regulator Topology for Low-Voltage Applications

Near-threshold computing has received significant attention due to enhanced energy efficiency, particularly for mobile systems-on-a-chip (SoCs) [36]. Highly parallelized architectures based on near-threshold operation have been proposed as a possible solution to dark silicon [37]. Developing an integrated voltage regulator module with application to near-threshold operation is challenging due to low output voltages in the range of 0.5 V. The regulator should simultaneously satisfy high power efficiency and power density (to minimize area overhead). Furthermore, the output ripple should be minimized since near-threshold circuits are highly sensitive to power supply variations (due to near-exponential dependence).

Hybrid regulators have also been developed to exploit the advantages of both LDOs and switching converters [38, 39], as conceptually depicted in Figure 3.8(a). Existing hybrid topologies, however, suffer in near-threshold

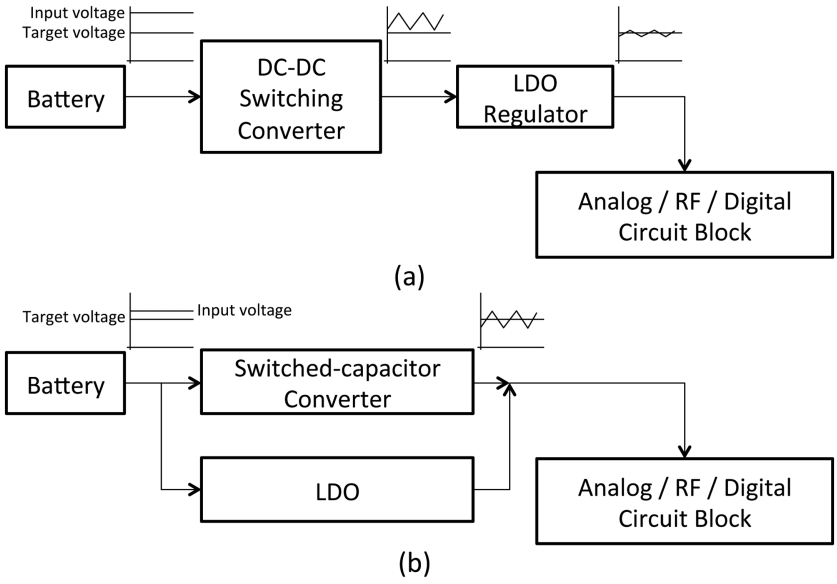

FIGURE 3.8
Conceptual block diagram of a (a) conventional hybrid regulator and a (b) proposed hybrid regulator.

operation, as further discussed in the following section. A novel hybrid topology, as shown in Figure 3.8(b), was developed [27]. This topology can produce low output voltages at high power efficiency. The proposed approach achieves approximately 85% power efficiency while supplying 100 mA output current at 0.5 V with a maximum ripple voltage of 22 mV.

3.3.1 Overview of Hybrid Regulator Topologies

In existing hybrid regulator approaches, a DC-DC switching converter is combined in series with an LDO, as shown in Figure 3.8(a) [38, 39]. The switched-capacitor circuit functions as a converter without any regulation capability, whereas the LDO regulates the output voltage without any conversion. Thus, the circuit enhances power efficiency since LDO has a near-unity voltage conversion ratio. Regulation is also enhanced due to an LDO with fast transient response at the output. Feed-forward ripple cancellation has also been proposed to further improve the regulation process [38]. This topology, however, suffers in near-threshold operation with large output current and low output voltage for three reasons:

- Power transistor of the LDO suffers from low $|V_{GS}|$ since the voltage conversion is achieved by the previous stage (switched-capacitor converter). This low input voltage makes it challenging to supply high current at the output.
- At high output current, the voltage drop across the power transistor (within an LDO) becomes nonnegligible, requiring a higher input voltage at the LDO. Higher input voltage, however, degrades the power efficiency.
- The maximum output load current cannot be larger than the current supplied by the switched-capacitor converter due to the series connection. Thus, the DC-DC switching converter needs to be optimized for the maximum load current rather than the nominal load current.

These limitations are exacerbated and the power efficiency is further degraded with reduced output voltages, as in near-threshold computing. Thus, a novel hybrid topology was proposed where the switched-capacitor converter and LDO operate in a parallel fashion, as conceptually illustrated in Figure 3.8(b). Specific design techniques are developed to ensure proper operation and outperform existing regulators, as discussed in the following section.

3.3.2 Proposed Regulator Topology Near-Threshold Computing

A simplified circuit schematic of the proposed hybrid regulator is shown in Figure 3.9. The switched-capacitor circuit and LDO operate in a parallel fashion where the source node of the power transistor within the LDO is

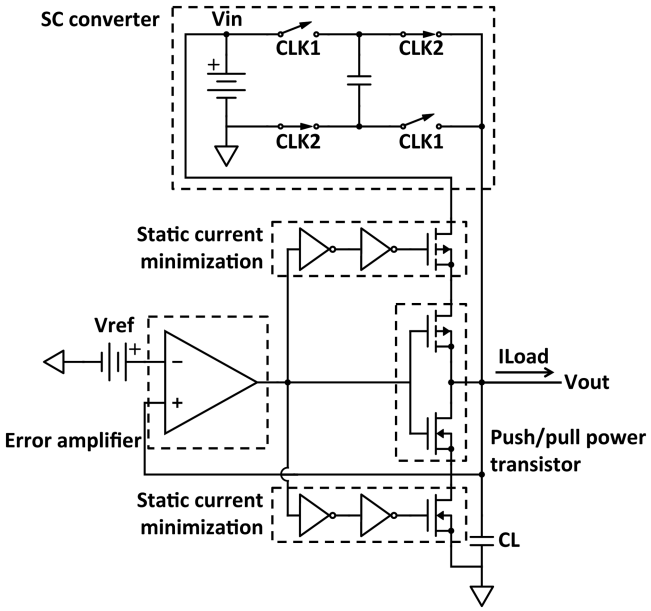

FIGURE 3.9
Proposed hybrid regulator consisting of an LDO (push/pull power transistors, error amplifier, and static current minimization) and switched-capacitor converter.

connected to the primary DC input voltage V_{in}. Thus, this topology does not suffer from the aforementioned limitations since LDO has a relatively larger input voltage. The switched-capacitor circuit provides the nominal output current while converting the input voltage from 1.15 to 0.5 V. At the nominal load current, LDO is turned off. Any variation at the output voltage is directly sensed by the error amplifier of the LDO, and output voltage is regulated with a fast transient response time. Some of the important characteristics of the proposed topology are

- No resistors are used within the LDO to minimize power loss.
- A static current minimization technique is developed to maximize power efficiency.
- Since the output voltage is directly sensed by the error amplifier, a small gain-bandwidth product is adopted, thereby preventing the output ripple from being amplified.

These characteristics are described in the following subsections.

3.3.2.1 Switched-Capacitor DC-DC Converter

A switched-capacitor converter consists of several switches and capacitors to achieve voltage conversion, as discussed in Section 3.2.2. The topology

shown in Figure 3.9 achieves a conversion ratio of 2, as typically required for near-voltage computing with existing technologies where the nominal supply voltages are in the range of 0.8–1 V and threshold voltages are in the range of 0.3–0.4 V. According to [40], the overall power loss can be expressed by

$$P_{loss} = P_{C_{fly}} + P_{R_{sw}} + P_{bott-cap} + P_{gate-cap}, \tag{3.5}$$

where $P_{C_{fly}}$, $P_{R_{sw}}$, $P_{bott-cap}$, and $P_{gate-cap}$ refer, respectively, to power loss due to flying capacitor, switch resistance, parasitic capacitance of flying capacitor, and that of the switches. $P_{C_{fly}}$ and $P_{R_{sw}}$ are

$$P_{R_{sw}} \propto I_L^2 \frac{R_{on}}{W_{sw}}, \quad P_{C_{fly}} \propto I_L^2 \frac{1}{C_{fly} f_{sw}}, \tag{3.6}$$

where I_L is the load current, R_{on} is the on resistance of a single switch, W_{sw} is the width of a single switch, C_{fly} is the flying capacitance, and f_{sw} is the switching frequency. The shunt power loss due to fully integrated flying capacitor $P_{bott-cap}$ and gate capacitance of the switches $P_{gate-cap}$ are

$$P_{bott-cap} \propto V_o^2 C_{bott} f_{sw}, \quad P_{gate-cap} \propto V_{sw}^2 C_{gate} f_{sw}, \tag{3.7}$$

where C_{bott} is the sum of the parasitic capacitance from the top and bottom plates of the flying capacitor, V_{sw} is the clock voltage swing, and C_{gate} is the gate capacitance of the switches. Following these expressions, the switch size and flying capacitor are determined to maximize power efficiency [40, 41]. These parameters are listed in Table 3.1.

3.3.2.2 Resistorless LDO

The proposed LDO does not contain any resistors to maximize power efficiency, as illustrated in Figure 3.9. Instead, a PMOS push power transistor provides the additional current to the load, whereas an NMOS pull transistor reduces the output voltage. These power transistors are controlled by the output of the error amplifier. The error amplifier directly senses the output voltage and adjusts its output based on the difference between the reference voltage and output voltage. Two important design characteristics are the

TABLE 3.1
Primary Parameters of the Switched-Capacitor Converter

W_{sw}/L_{sw}	43×25 μm/50 nm
C_{fly}	1.5 nF
C_L	1.5 nF
Switching frequency	482 MHz

error amplifier and the static current minimization technique, as described in the following subsections.

3.3.2.3 Optimization of the Error Amplifier

In conventional LDOs, the output frequency spectrum is determined solely by the error amplifier within the LDO. Alternatively, in the proposed regulator, the high-frequency components of the output frequency spectrum, as depicted in Figure 3.10, are dominantly determined by the switched-capacitor converter since it operates in parallel with the LDO. As listed in Table 3.1, the switching frequency is 482 MHz. According to Figure 3.10, the output voltage has a strong frequency component at this switching frequency, demonstrating the effect of the switched capacitor on the frequency spectrum. Thus, the ripple at the output voltage is primarily determined by the switched capacitor. This behavior is important since the error amplifier directly senses the output voltage in this approach. To prevent the error amplifier from amplifying output ripple, the gain-bandwidth product should be smaller than the switching frequency of the switched-capacitor circuit. Note, however, that a sufficiently small gain-bandwidth product slows down the circuit, increasing the response time. Considering this trade-off, the gain-bandwidth product is determined as approximately 350 MHz.

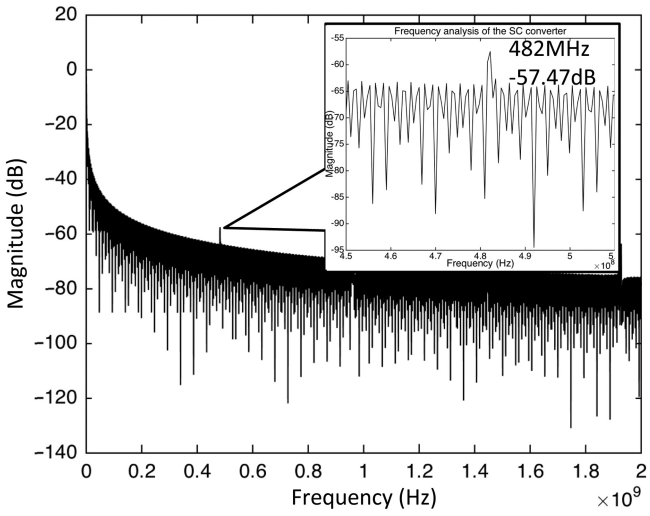

FIGURE 3.10
Frequency spectrum of the output voltage with 100 mA current.

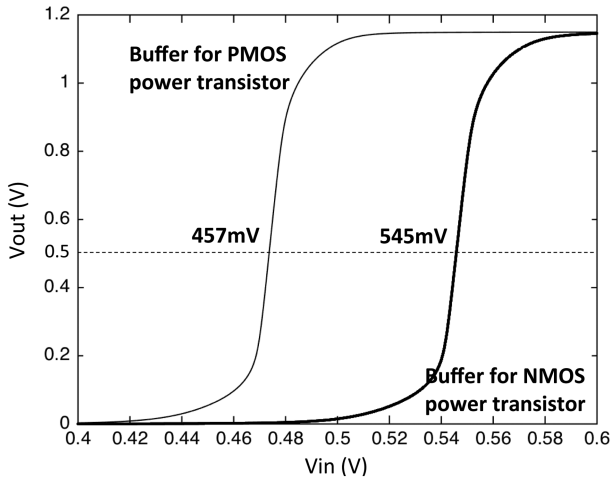

FIGURE 3.11
DC analysis of the buffers added to prevent static current.

3.3.2.4 Static Current Minimization

As opposed to traditional LDOs with single PMOS power transistor, the proposed LDO consists of both PMOS and NMOS power transistors to be able to increase and decrease the output voltage during regulation. Thus, according to the error amplifier output, both power transistors can be on, dissipating significant static current. This behavior should be prevented to maximize power efficiency. For this reason, a buffer with a different switching voltage is added before each power transistor, as illustrated in Figure 3.9. The DC voltage characteristics of these buffers are shown in Figure 3.11. As illustrated in this figure, the buffer preceding the PMOS power transistor has a much smaller switching voltage than the buffer preceding the NMOS power transistor. This difference in the switching voltage ensures that either (1) only PMOS power transistor is on or (2) only NMOS power transistor is on or both (3) power transistors are off. The difference in the switching voltages is determined to ensure that the situation when both transistors are on is avoided, thereby preventing the static current.

3.3.3 Simulation Results

The proposed novel hybrid regulator is designed using a 45 nm complementary metal-oxide semiconductor (CMOS) technology with a capacitance density of 30 nF/mm^2. The input voltage is 1.15 V and the output voltage is 0.5 V, which is slightly larger than the threshold voltage. The nominal load current

is 100 mA, as supplied by the switched-capacitor converter. The total capacitance is 3 nF, which approximately occupies 0.1 mm^2, thereby achieving approximately 0.5 W/mm^2. As recently demonstrated by [42], regulators for portable SoCs require this power density to ensure proper operation at reasonable cost.

The output voltage and error amplifier output are plotted in Figure 3.12 when the load current varies from 65 to 130 mA. As illustrated in this figure, the output of the error amplifier is reduced as the load current increases. Thus, additional current is supplied by the PMOS power transistor. Output voltage remains approximately at 0.5 V with a maximum ripple of 22 mV.

The power efficiency is plotted in Figure 3.13 as a function of load current. At the nominal load of 100 mA, the regulator achieves approximately 85% power efficiency. Note that the power efficiency is maintained above

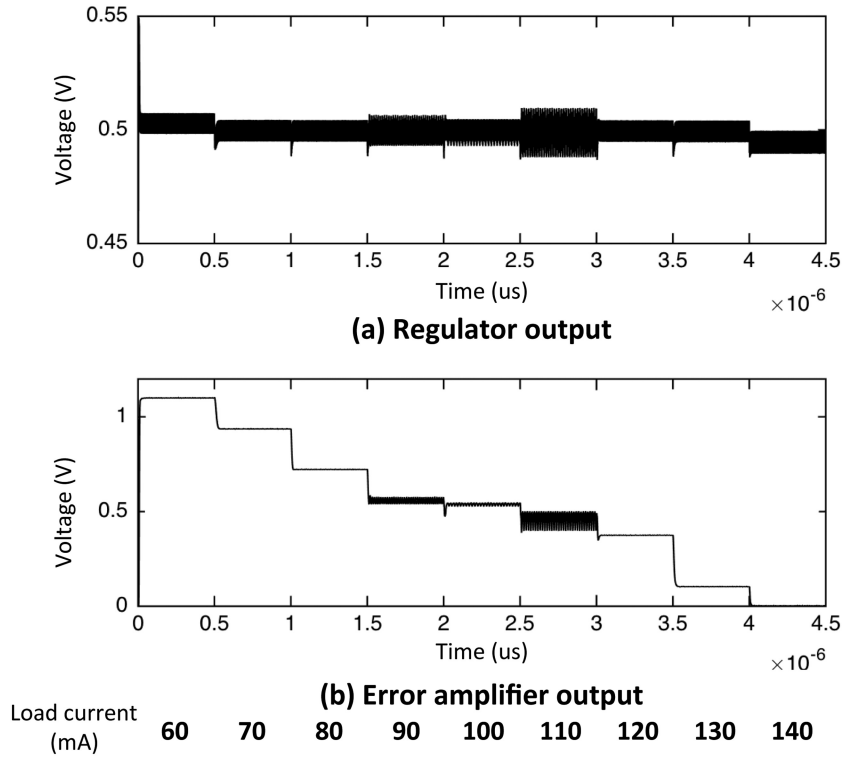

FIGURE 3.12
Simulation results as the load current abruptly changes from 60 to 140 mA with a step size of 10 mA: (a) output voltage of the regulator and (b) output voltage of the error amplifier.

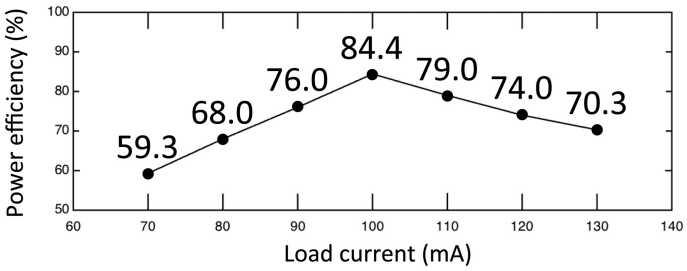

FIGURE 3.13
Power efficiency of the proposed regulator.

70% across a relatively broad range of load current, from approximately 82 to 130 mA.

Finally, the transient response of the proposed regulator is depicted in Figure 3.14. When the load current changes from 65 to 130 mA, the regulator requires approximately 18 ns to regulate the output voltage back to 0.5 V. Alternatively, when the load current changes from 130 to 65 mA, the regulator responds more quickly with a response time of 10 ns. The maximum overshoot and undershoot are less than 50 mV in both cases.

The proposed regulator is compared with several recent existing works, developed for similar applications. The comparison results are listed in Table 3.2. According to this table, at comparable current density, this work outperforms other works in both power efficiency and output ripple. Specifically, the output ripple is reduced by more than 60%, enabling a more robust near-threshold operation. A reasonable transient response time is also achieved.

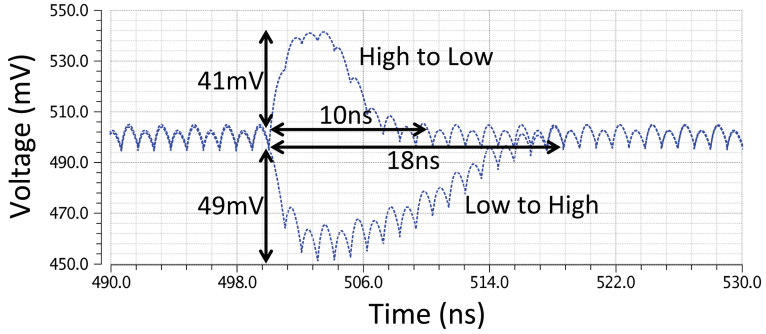

FIGURE 3.14
Transient response of the proposed regulator when the load current abruptly changes.

TABLE 3.2
Comparison of the Proposed Regulator with Existing Work

Reference	H.-P. Le 2013 [43]	R. Jain 2014 [44]	M. Abdelfattah 2015 [45]	This work
Technology	65 nm	22 nm trigate	45 nm SOI	45 nm
Input voltage	3–4 V	1.23 V	1.15 V	1.15 V
Output voltage	1 V	0.45–1 V @ 88 mA	0.5 V @ 5–125 mA	0.5 V @ 65–130 mA
Power efficiency	73%	70%@ 0.55 V 84%@ 1.1 V	74–80% @ 5–125 mA	84.4% @ 100 mA
Response time	N/A	3–5 ns	3–95 ns	<20 ns
Current density	0.19 A/mm^2	0.88 A/mm^2	1.25 A/mm^2	1 A/mm^2
Ripple voltage	N/A	60 mV	62 mV	Max: 22 mV Min: 9 mV

3.4 Summary and Conclusions

The significant opportunities and fundamental challenges related to monolithic voltage regulators have been discussed in this chapter. An overview of primary voltage regulator topologies such as linear dropout, switched-capacitor-based, and switching buck regulators has been provided. A qualitative comparison of these topologies was also considered to describe design trade-offs related to on-chip integration.

In the second part of this chapter, a novel hybrid regulator topology was described with application to near-threshold computing in portable SoCs. Contrary to existing approaches, a switched-capacitor converter and an LDO operate in a parallel fashion to convert and regulate the output voltage. The proposed LDO does not contain any resistors to minimize power loss. A static current minimization technique has also been introduced to maximize power efficiency. The error amplifier within the LDO is optimized by appropriately choosing the gain-bandwidth product, thereby minimizing the output ripple.

The primary emphasis is on maximizing power efficiency while maintaining sufficient regulation capability (with ripple voltage less than 5% of the output voltage) and power density. Simulation results in 45 nm technology demonstrate a power efficiency of approximately 85% at 100 mA load current with an input and output voltage of, respectively, 1.15 and 0.5 V. The worst-case transient response time is under 20 ns when the load current varies from 65 to 130 mA. The worst-case ripple is 22 mV while achieving a power density of 0.5 W/mm^2.

References

1. E. Salman and E. G. Friedman, *High Performance Integrated Circuit Design*, McGraw Hill Professional, 2012.
2. G. Semeraro et al., "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," *Proceedings of the IEEE International Symposium on High-Performance Computer Architecture*, pp. 29–40, Feb. 2002.
3. C. Sitik, W. Liu, B. Taskin, and E. Salman, "Design Methodology for Voltage-Scaled Clock Distribution Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 10, No. 24, pp. 3080–3093, 2016.
4. V. Kursun and E. G. Friedman, *Multi-Voltage CMOS Circuit Design*, John Wiley & Sons, 2006.
5. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Worst Case Power/Ground Noise Estimation Using an Equivalent Transition Time for Resonance," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 56, No. 5, pp. 997–1004, May 2009.
6. E. Salman, E. G. Friedman, and R. M. Secareanu, "Substrate and Ground Noise Interactions in Mixed-Signal Circuits," *Proceedings of the IEEE International SoC Conference*, pp. 293–296, Sept. 2006.
7. H. Wang and E. Salman, "Closed-Form Expressions for I/O Simultaneous Switching Noise Revisited," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, pp. 769–773, Feb. 2017.
8. Z. Gan, E. Salman, and M. Stanacevic, "Figures-of-Merit to Evaluate the Significance of Switching Noise in Analog Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 23, pp. 2945–2956, Dec. 2015.
9. E. A. Burton et al., "FIVR—Fully Integrated Voltage Regulators on 4th Generation Intel Core SoCs," *Proceedings of IEEE Applied Power Electronics Conference and Exposition*, pp. 432–439, 2014.
10. V. Kursun, S. G. Narendra, V. K. De, and E. G. Friedman, "Efficiency Analysis of a High Frequency Buck Converter for On-Chip Integration with a Dual-V_{DD} Microprocessor," *Proceedings of the IEEE European Solid-State Circuits Conference*, pp. 743–746, Sept. 2002.
11. V. Kursun, S. G. Narendra, V. K. De, and E. G. Friedman, "Analysis of Buck Converters for On-Chip Integration with a Dual Supply Voltage Microprocessor," *IEEE Transactions on Very Large Scale Integration Systems*, Vol. 11, No. 3, pp. 514–522, 2003.
12. T. Simunic et al., "Dynamic Voltage Scaling and Power Management for Portable Systems," *Proceedings of the IEEE/ACM Design Automation Conference*, pp. 524–529, June 2001.
13. W. Kim, M. S. Gupta, G. Y. Wei, and D. M. Brooks, "Enabling On-Chip Switching Regulators for Multi-Core Processors Using Current Staggering," *Proceedings of the Workshop on Architectural Support for Gigascale Integration*, June 2007.
14. G. Patounakis, Y. W. Li, and K. Shepard, "A Fully Integrated On-Chip DC-DC Conversion and Power Management System," *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 3, pp. 443–451, Mar. 2004.

15. K. N. Leung and P. K. T. Mok, "A Capacitor-Free CMOS Low-Dropout Regulator with Damping-Factor-Control Frequency," *IEEE Journal of Solid-State Circuits*, Vol. 37, No. 10, pp. 1691–1701, Oct. 2003.
16. R. K. Dokaniz and G. A. Rincon-Mora, "Cancellation of Load Regulation in Low Drop-Out Regulators," *Electronics Letters*, Vol. 38, No. 22, pp. 1300–1302, Oct. 2002.
17. C. K. Chava and J. Silva-Martinez, "A Robust Frequency Compensation Scheme for LDO Voltage Regulators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 51, No. 6, pp. 1041–1050, June 2004.
18. G. A. Rincon-Mora and P. E. Allen, "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 1, pp. 36–44, Jan. 1998.
19. P. Hazucha et al., "Area-Efficient Linear Regulator with Ultra-Fast Load Regulation," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 4, pp. 933–940, Apr. 2005.
20. D. Maksimovic and S. Dhar, "Switched-Capacitor DC-DC Converters for Low-Power On-Chip Applications," *Proceedings of the IEEE Power Electronics Specialists Conference*, pp. 54–59, June 1999.
21. A. Chandrakasan and R. W. Brodersen, *Low Power CMOS Digital Design*, Kluwer Academic Publishers, 1995.
22. D. Baba, "Benefits of a Multiphase Buck Converter," *Analog Applications*, pp. 8–13, 2012.
23. X. Zhou et al., "Investigation of Candidate VRM Topologies for Future Microprocessors," *IEEE Transactions on Power Electronics*, Vol. 15, No. 6, pp. 1172–1182, 2000.
24. J. Clarkin, "Design of a 50A Multi-Phase Converter," *Proc. Conf. Rec., HFPC*, pp. 414–420, 1999.
25. W. Kim, M. S. Gupta, G. Y. Wei, and D. Brooks, "System Level Analysis of Fast, Per-Core DVFS Using On-Chip Switching Regulators," *Proceedings of IEEE Symposium on High Performance Computer Architecture*, pp. 123–134, 2008.
26. Z. Toprak et al., "5.2 Distributed System of Digitally Controlled Microregulators Enabling Per-Core DVFS for the POWER8 TM Micro- processor," *Proceedings of IEEE International Solid-State Circuits Conference*, pp. 98–99, 2014.
27. Y. Park and E. Salman, "On-Chip Hybrid Regulator Topology for Portable SoCs with Near-Threshold Operation," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 786–789, 2016.
28. C. Huang and P. Mok, "An 84.7% Efficiency 100-MHz Package Bondwire-Based Fully Integrated Buck Converter with Precise DCM Operation and Enhanced Light-Load Efficiency," *IEEE Journal of Solid-State Circuits*, Vol. 48, No. 11, pp. 2595–2607, 2013.
29. Y. Ahn, H. Nam, and J. Roh, "A 50-MHz Fully Integrated Low-Swing Buck Converter Using Packaging Inductors," *IEEE Transactions on Power Electronics*, Vol. 27, No. 10, pp. 4347–4356, 2012.
30. S. A. Chickamenahalli et al., "RF Packaging and Passives: Design, Fabrication, Measurement, and Validation of Package Embedded Inductors," *IEEE Transactions on Advanced Packaging*, Vol. 28, No. 4, pp. 665–673, 2005.
31. C. Yan, Z. Gan, and E. Salman, "Package Embedded Spiral Inductor Characterization with Application to Switching Buck Converters," *Microelectronics Journal*, Vol. 66, pp. 41–47, Aug. 2017.

32. C. Yan, Z. Gan, and E. Salman, "In-Package Spiral Inductor Characterization for High Efficiency Buck Converters," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2396–2399, May 2017.
33. K. Onizuka et al., "Stacked-Chip Implementation of On-Chip Buck Converter for Distributed Power Supply System in SiPs," *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 11, pp. 2404–2410, 2007.
34. J. Wibben and R. Harjani, "A High-Efficiency DC-DC Converter Using 2 nH Integrated Inductors," *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 4, pp. 844–854, 2008.
35. S. S. Kudva and R. Harjani, "Fully-Integrated On-Chip DC-DC Converter with a 450X Output Range," *IEEE Journal of Solid-State Circuits*, Vol. 46, No. 8, pp. 1940–1951, 2011.
36. R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-Threshold Computing: Reclaiming Moore's Law through Energy Efficient Integrated Circuits," *Proceedings of the IEEE*, Vol. 98, No. 2, pp. 253–266, Feb. 2010.
37. B. Zhai, R. G. Dreslinski, D. Blaauw, T. Mudge, and D. Sylvester, "Energy Efficient Near-threshold Chip Multi-processing," *ACM/IEEE Int. Symp. on Low Power Electronics and Design*, pp. 32–37, Aug. 2007.
38. M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sanchez-Sinencio, "High PSR Low Drop-Out Regulator with Feed-Forward Ripple Cancellation Technique," *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 3, pp. 565–577, Mar. 2010.
39. K. K. G. Avalur and S. Azeemuddin, "Automotive Hybrid Voltage Regulator Design with Adaptive LDO Dropout Using Load-sense Technique," *IEEE Asia Pacific Conf. on Circuits and Syst.*, pp. 571–574, Nov. 2014.
40. H.-P. Le, S. R. Sanders, and E. Alon, "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," *IEEE Journal of Solid-State Circuits*, Vol. 46, No. 9, pp. 2120–2131, Sept. 2011.
41. M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," *IEEE Workshops on Computers in Power Electronics*, pp. 216–224, July 2006.
42. L. G. Salem and P. P. Mercier, "A Footprint-constrained Efficiency Roadmap for On-chip Switched-capacitor DC-DC Converters," *IEEE Int. Symp. on Circuits and Systems*, pp. 2321–2324, May 2015.
43. H. P. Le, J. Crossley, S. R. Sanders, and E. Alon, "A Sub-ns Response Fully Integrated Battery-connected Switched-capacitor Voltage Regulator Delivering 0.19W/mm^2 at 73% efficiency," *IEEE Int. Solid-State Circuits Conf.*, pp. 372–373, Feb. 2013.
44. R. Jain, B. M. Geuskens, S. T. Kim, M. M. Khellah, J. Kulkarni, J. W. Tschanz, and V. De, "A 0.45-1 V Fully-Integrated Distributed Switched Capacitor DC-DC Converter with High Density MIM Capacitor in 22 nm Tri-Gate CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 49, No. 4, pp. 917–927, Apr. 2014.
45. M. Abdelfattah, B. Dupaix, S. Naqvi, and W. Khalil, "A Fully-integrated Switched Capacitor Voltage Regulator for Near-threshold Applications," *IEEE Int. Symp. on Circuits and Systems*, pp. 201–204, May 2015.