Emre Salman

Contact Information

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Electrical and Computer Engineering
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Research Interests

- Integrated circuits and VLSI systems with applications to
  - Energy-efficient and secure computing
  - Internet-of-things with energy harvesting
  - Implantable electronics for healthcare
- Emerging integrated circuit and system technologies

Education

University of Rochester, Rochester, New York USA

Ph.D., Electrical Engineering, May 2009

- Advisor: Eby G. Friedman

M.S., Electrical and Computer Engineering, May 2006

Sabanci University, Istanbul, Turkey

B.S., Microelectronics Engineering, July 2004

Professional Experience

Stony Brook University (SUNY), Stony Brook, New York USA

Professor — **September, 2023 - present**
Electrical and Computer Engineering

Associate Professor — **September, 2016 - August 2023**
Electrical and Computer Engineering

Director — **September, 2011 - present**
Nanoscale Circuits and Sysems (NanoCAS) Laboratory

Assistant Professor — **September, 2010 - August, 2016**
Electrical and Computer Engineering

Air Force Research Labs, Rome, New York

Visiting Faculty Research Fellow — **May, 2021 - July, 2021**

Sabanci University, Istanbul, Turkey

Visiting Professor — **January, 2020 - June, 2020**
Faculty of Engineering and Natural Sciences

University of Rochester, Rochester, New York USA

Post-doctoral Research Associate — **June, 2009 - August, 2010**
Electrical and Computer Engineering

Instructor — **January, 2010 - July, 2010**
Rochester Scholars Program

Freescale Semiconductor, Tempe, Arizona USA

Graduate Intern **Summer 2006 and 2007**
Microwave and Mixed-Signal Technologies

Synopsys, Mountain View, California USA

Graduate Intern **Summer 2005**
PrimeTime Static Timing Analysis Group

STMicroelectronics, Istanbul, Turkey

IC Design Intern **September, 2003 - June, 2004**
Analog and Mixed-Signal Team

Honors and Awards

- **Distinguished Lecturer**, IEEE Circuits and Systems Society, 2023-2024
  - Talk 1: Charge-Recycling based Design Paradigm for Efficient and Secure RF-Powered IoT Devices
  - Talk 2: Thermal-Centric Design Methodologies for Monolithic 3D Integrated Circuits
- **Inductee of National Academy of Inventors**, Stony Brook Chapter, April 2021
  - NAI membership "recognizes the contributions of scientist-inventors across all disciplines."
- **Technological Innovation Award**, IEEE Region 1, September 2018
  - Citation, "for outstanding contributions to developing energy-efficient and secure 3D ICs."
- **Stony Brook University Inaugural Leadership Academy Fellow**, Spring 2018
  - Selected from a pool of associate professors across the university, nominated by departmental chairs. The fellows participated in various leadership workshops.
- **Best Paper Award**, Semiconductor Research Corporation (SRC) TECHCON, September 2016
  - W. Liu, C. Sitik, E. Salman, B. Taskin, S. Sundareswaran, and B. Huang, "Slew-Driven Clock Tree Synthesis Methodology to Facilitate Low Voltage Clocking," *SRC Technology Conference (TECHCON)*, September 2016
- **SUNY Inaugural Discovery Fund Prize Finalist**, December 2014
  - For research on AC computing methodology for wirelessly-powered devices
  - "The Discovery Fund is Stony Brook University's response to a nationwide call to augment public funding of university research with philanthropic support with emphasis on high risk, high reward research addressing modern problems."
- **IEEE Long Island Outstanding Young Engineer Award**, March 2014
  - "This award honors a Long Island IEEE member who has made important technical contributions prior to his or her 35^{th} birthday."
- **National Science Foundation (NSF) CAREER Award**, March 2013
  - For research on "leveraging 3D integration technology for highly heterogeneous SoCs"
- **IEEE Circuits and Systems Society, Outreach Initiative Award**, 2012, 2013, 2015, 2017
  - For organizing high impact outreach activities in Long Island, New York

Selected Media Coverage

- $2.3 million NIH grant to fund research on smart knee replacements, June 2022
  - https://www.eurekalert.org/news-releases/956363
- Smart, Self-Powered Knee Implants Could Reduce Knee Replacement Surgeries, Jan. 2019
  - https://www.eurekalert.org/news-releases/658039
- Wireless Energy Harvesting for IoT Devices, March 2017
  - https://sciencenode.org/feature/wireless-energy-harvesting-for-iot-devices.php
- Stony Brook Discovery Fund Challenge Held at Simons Foundation, Jan. 2015
  - https://www.simonsfoundation.org/features/foundation-news/stony-brook-discovery-fund-challenge-held-at-simons-foundation/
- Stony Brook Announces Four Finalists for Inaugural Discovery Fund Award, Nov. 2014
  - http://www.labmanager.com/news/2014/11/stony-brook-announces-four-finalists-for-inaugural-discovery-fund-award
- Scientist developing 3-D chips to expand capacity of microprocessors, Jan. 2014
  - https://new.nsf.gov/news/scientist-developing-3-d-chips-expand-capacity
- Smaller, better, faster, stronger 3D chips, April 2014
  - https://sciencenode.org/spotlight/smaller-better-faster-stronger-3d-chips.php
- New Research Advances Heterogeneous 3D Chip Design, Feb. 2014
  - http://www.hpcwire.com/2014/02/06/researcher-advances-heterogenous-3d-chip-design/

Grants and Contracts

1. Stony Brook University - Brookhaven National Laboratory Seed Grant Program, "Next-Generation Diagnostic Tests for Radiation Tolerant AI Hardware," $94,240, Co-PI, 9/2024-2/2026, with P. Milder (PI), T. Robertazzi, and X. Jiang (BNL)

2. SUNY Resubmission Grant, "Thermal-Centric Co-Design Methodologies for Monolithic 3D Integrated DNN Accelerators," $40,000, PI, 6/2024-11/2025

3. Stony Brook University - Brookhaven National Laboratory Seed Grant Program, "Self-Healing Wireline Transceivers with Embedded Intelligence for Extreme Environments," $90,000, PI at Stony Brook, 7/2023-12/2024, with N. St. John (BNL) and S. Mandal (BNL)

4. Office of the Vice President for Research (OVPR) at Stony Brook University, "Energy-Efficient Design Methodologies for ReRAM-based Deep Neural Network Accelerators on the Edge," $50,000, PI, 8/2022-2/2024, with M. Stanacevic

5. National Institute of Health (NIH), "Self-Powered Load Sensors for Total Knee Replacement Health Monitoring," $890,000, PI, 06/22-05/27, with M. Stanacevic, sub-award from Binghamton University

6. National Science Foundation (NSF), "CPS: Medium: Collaborative Research: Scalable Intelligent Backscatter-Based RF Sensor Network for Self-Diagnosis of Structures," $799,863, Co-PI, 10/2021-9/2024, with P. Djuric (PI), M. Stanacevic, and S. Das

7. Saniteq LLC, "Design and Construction of a Field Testable Dielectric Multiphase Flowmeter," $21,220, PI, 9/20/19-1/20/20

8. National Science Foundation (NSF), "SHF: Small: Collaborative Research: Managing Thermal Integrity in Monolithic 3D Integrated Systems," $500,000, Lead PI, 7/2019-6/2022, with A. Coskun from Boston University

9. SUNY Center-Scale Proposal Planning and Development Grant Program, "CEINTS: Center for Engineering INtelligent Tag NetworkS," $50,000, Co-PI, 07/2018-06/2019, with S. Das, P. Djuric, and M. Stanacevic
10. National Science Foundation (NSF) and Semiconductor Research Corporation (SRC) Joint Funding, "SaTC: STARSS: Small: Collaborative: Managing Hardware Security in Three-Dimensional Integrated Circuits," $450,000, PI at Stony Brook, 10/2017-9/2020, with Q. Yu from University of New Hampshire
11. National Institute of Health (NIH), "An Implantable Self-Powered Load Sensor for Total Knee Replacement Health Monitoring," $112,824, PI at Stony Brook, 9/2017-8/2019, sub-award from Binghamton University
12. National Science Foundation (NSF), "CPS: Breakthrough: Charge-Recycling based Computing Paradigm for Wirelessly Powered Internet-of-Things," $425,000, PI, 9/2016-8/2019, with M. Stanacevic
13. Public Service Enterprise Group, "Stony Brook Inspiring Engineering Learning Program," $150,000, Co-PI, 9/2015-8/2018, with. M. Bugallo
14. Simons Foundation, "New Milestone in Energy Autonomy: Novel Charge-Recycling Circuits for Wireless Power Harvesting," $50,000 (gift), PI, 11/2014-12/2017, with M. Stanacevic
15. Semiconductor Research Corporation (SRC), "Design and Automation of a Novel Low Swing Clocking Methodology with Reduced Delay Uncertainty," $225,000, PI/PD, 10/2013-3/2017 (with B. Taskin)
16. Office of the Vice President for Research (OVPR) at Stony Brook University, "CAREER: Leveraging Three-Dimensional Integration Technology for Highly Heterogeneous Systems-on-Chip," $35,000, PI, 7/2013-6/2018
17. National Science Foundation (NSF), "CAREER: Leveraging Three-Dimensional Integration Technology for Highly Heterogeneous Systems-on-Chip," $453,809, PI, 3/2013-2/2018
18. IEEE Circuits and Systems Society, "Outreach Activities for High School Students: Educating Electrical Engineers of the Future," $21,300, PI, 10/2012-9/2017

Invited Talks Tutorials

- Sustainable Microelectronics in the Age of AI, Invited Talk at the AVS International Symposium and Exhibition, Tampa, FL, November 2024
- Thermal-Centric Design Methodologies for Monolithic 3D Integrated Circuits, Aristotle University Thessaloniki (AUTH), Greece, October 2024
- Circuits and Devices for Edge AI, Invited Talk at High Energy Physics Integrated Circuits Workshop, Brookhaven National Laboratory, May 2024
- Thermal-Centric Design Methodologies for Monolithic 3D Integrated Circuits, IEEE Princeton Central Jersey Section and Rutgers University, New Jersey, March 2024
- Charge-Recycling based Design Paradigm for Efficient and Secure RF-Powered IoT Devices, IEEE Southeastern Michigan Chapter, Michigan, December 2023
- Energy-Efficiency in the Post-Moore Era: Challenges and Opportunities, Brookhaven National Laboratory, October 2023
- Energy-Efficient DNN Accelerators in the Post-Moore Era: Challenges and Opportunities, Fall Seminar Series at Department of Electrical and Computer Engineering, University of Delaware, October 2023
- Charge-Recycling based Design Paradigm for Efficient and Secure RF-Powered IoT Devices, IEEE Tainan Section Chapter, Taiwan, April 2023
- Charge-Recycling based Design Paradigm for Efficient and Secure RF-Powered IoT Devices, Architecture and Circuit Research Center (ACRC), Technion, Israel, February 2023

- Leveraging Monolithic 3D Technology for Data-Centric Applications, Workshop on EES2 (Energy Efficiency Scaling Goal), Advanced Manufacturing Office, Department of Energy, September 2022
- Accuracy- and Performance-Aware Voltage Scaling Strategies for DNN Accelerators, Instrumentation Division, Brookhaven National Laboratory, Brookhaven, NY, August 2022
- Error-Aware Deep Neural Network Accelerators Operating at Low Voltages, Information Institute Tech Talks at Air Force Research Labs, Rome, NY, August 2021
- Hardware Security in Three-Dimensional Integrated Circuits and Systems, October 2020
  - Mini tutorial at IEEE International Symposium on Circuits and Systems
- Recent Advances on Monolithic 3D Integrated Circuits, The National Synchrotron Light Source II, Brookhaven National Laboratory, Brookhaven, NY, October 2019
- Potential of AC Computing for IoT and Beyond, Google Inc., Sunnyvale, CA, September 2018
- Back to the "War of Currents": Can AC Computing be an Alternative for Wirelessly Powered Devices?, Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY, May 2017
- Low Voltage Clocking as a Practical Low Power Design Strategy for Industrial Circuits, Samsung Austin Research Center (SARC), Austin, TX, November 2016
- VLSI Design Beyond 50^{th} Anniversary of Moore's Law, Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, NY, September 2016
- Design and Automation of a Novel Low Swing Clocking Methodology with Reduced Delay Uncertainty, Semiconductor Research Corporation Design Review, Dallas, TX, November 2015
- Circuits and Algorithms to Facilitate Low Swing Clocking in Nanoscale Technologies, September 2015
  - Advanced Micro Devices (AMD) Inc., Austin, TX
  - Freescale Semiconductor Inc. (Now NXP Semiconductors), Austin, TX
- Low Voltage Power Delivery and Clocking in Nanoscale Technologies: Basics to Recent Advances, Lisbon, Portugal, May 2015
  - Three-hour long tutorial at IEEE International Symposium on Circuits and Systems
- Challenges and Opportunities in 3D Integrated Circuits, IEEE Long Island, Farmingdale, NY, April 2015
- New Milestony in Wireless Energy Harvesting, Simon's Foundation, New York, NY, December 2014
  - TED-type talk to a diverse audience of over 100 people and distinct judges including Nobel laureate Peter Agre for 2014 Discovery Prize Competition
- Design and Automation of a Novel Low Swing Clocking Methodology with Reduced Delay Uncertainty, Semiconductor Research Corporation Design Review, UC Berkeley, CA, October 2014.
- Ensuring Power and Signal Integrity in Heterogeneous 3D ICs, Workshop on 2.5D/3D Technology and Design Enablement for Heterogeneous Systems, Nanyang Technological University, Singapore, July 2013
- Robust Power Delivery in TSV Based 3D Processor-Memory Stacks, CASS Forum on Emerging and Selected Topics (CAS-FEST), Heterogeneous Nano-Circuits and Systems, Seoul, South Korea, May 2012

PUBLICATIONS

- **Book**

1. E. Salman and E. G. Friedman, *High Performance Integrated Circuit Design*, McGraw-Hill, ISBN:0071635769, September 2012
   - Comprehensive tutorial book that unifies interconnect-centric design methodologies
   - Adopted as a textbook for graduate level courses at multiple higher education institutions
2. E. Salman and E. G. Friedman, 高性能集成电路设计, Electronic Industry Press, ISBN 7121250903, January 2015 (Chinese Translation)

- **Patents**

1. R. Willing, E. Salman, M. Stanacevic, M. Jain, S. Towfighian N. A. Hossain, I. Alwatiqbellah, "Self-Powered Load Sensing Circuitry for Total Knee Replacement," US Patent Pending
2. E. Salman, M. Stanacevic, T. Wan, Y. Karimi, and Y. Huang, "Ultra Low Power Core for Lightweight Encryption," US Patent No US11838402B2
3. E. Salman, M. Stanacevic, T. Wan, and Y. Karimi, "Radio Frequency (RF) Energy Harvesting and Method for Utilizing the Same," US Patent No US10846581B2
4. B. Taskin, C. Sitik, E. Salman, and W. Liu, "Slew-Aware Clock Tree Synthesis," US Patent No 103,386,33B2
5. A. Dasdan, E. Salman, F. Taraporevala, and K. Kucukcakar, "Characterizing Sequential Cells Using Interdependent Setup and Hold Times, and Utilizing the Sequential Cell Characterization in Static Timing Analysis," US Patent No 7,506,293
6. R. M. Secareanu, O. L. Hartin, and E. Salman, "Apparatus and Method For Reducing Noise in Mixed-Signal Circuits and Digital Circuits," US Patent No 7,834,428

- **Invited Book Chapters**

1. E. Salman, "On-Chip Regulators for Low Voltage and Portable Systems-on-Chip," *Energy Efficient Technologies: Devices, Circuits, and Systems*, pp. 57-79, S. Kurinec and K. Iniewski (Eds.), CRC Press, February 2019
2. E. Salman, "Overview of Substrate Induced Signal Integrity in 2D and 3D ICs," *Noise Coupling in System-on-Chip*, T. Noulis (Ed.), CRC Press, pp. 21-44, T. Noulis (Ed.), CRC Press, December 2017
3. E. Salman, "Power and Signal Integrity Challenges in 3D Systems-on-Chip," *Physical Design for 3D Integrated Circuits*, pp. 101-126, A. Todri-Sanial and C. S. Tan (Eds.), CRC Press, December 2015
4. M. Stanacevic, Y. Lin, and E. Salman, "Analysis and Design of 3D Potentiostat for Deep Brain Implantable Devices," *Neural Computation, Neural Devices, and Neural Prosthesis*, pp. 261-287, Z. Yang (Ed.), Springer, 2014

- **Journal Papers**

1. M. Chahari, H. Haghshenas, E. Salman, M. Stanacevic, R. Willing and S. Towfighian, "Towards Self-Powered Load Imbalance Detection for Instrumented Knee Implants Using Quadrant Triboelectric Energy Harvesters," *IEEE Sensors Journal*, Vol. 24, No. 12, November 2024
2. M. Chahari, E. Salman, M. Stanacevic, R. Willing, and S. Towfighian, "Hybrid triboelectric-piezoelectric nanogenerator for long-term load monitoring in total knee replacements," *Smart Materials and Structures*, Vol. 33, No. 5, April 2024
3. I. Miketic and E. Salman, "PowerID: Using Supply-Side Impedances of Power Delivery Networks as Signatures for Consumer Electronics," *IEEE Transactions on Consumer Electronics*, Vol. 70, No. 1, February 2024

4. P. Shukla, V. Pavlidis, E. Salman, A. Coskun, "TREAD-M3D: Temperature-Aware DNN Accelerators for Monolithic 3D Mobile Systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 42, No. 12, December 2023
5. I. Miketic, K. Dhananjay, and E. Salman, "Perspective Paper: Covert Channel Communication as an Emerging Security Threat in 2.5/3D Integrated Systems," *Sensors*, Vol. 23, No. 4, February 2023
6. K. Dhananjay and E. Salman, "SEAL-RF: SEcure Adiabatic Logic for Wirelessly-Powered IoT Devices," *IEEE Internet-of-Things Journal*, Vol. 10, No. 2, pp. 1112-1123, January 2023
7. K. Dhananjay, V. Pavlidis, A. Coskun, and E. Salman, "High Bandwidth Thermal Covert Channel in 3D-Integrated Multicore Processors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 30, No. 11, pp. 1654-1667, November 2022
8. M. Jain, N. A. Hossain, S. Towfighian, R. Willing, M. Stanacevic, and E. Salman, "Self-Powered Load Sensing Circuitry for Total Knee Replacement," *IEEE Sensors*, Vol. 21, No. 20, pp. 22967-22975, October 2021
9. I. Miketic and E. Salman, "PhaseCamouflage: Leveraging Adiabatic Operation to Thwart Reverse Engineering," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 29, No. 7, pp. 1285-1296, July 2021
10. K. Dhananjay and E. Salman, "Charge Based Power Side-Channel Attack Methodology for an Adiabatic Cipher," *Electronics*, Vol. 10, No. 12, pp. 1438-1454, June 2021
11. K. Dhananjay, P. Shukla, V. Pavlidis, A. Coskun, and E. Salman, "Monolithic 3D Integrated Circuits: Recent Trends and Future Prospects," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 68, No. 3, pp. 837 - 843, March 2021
12. M. Rathore, P. Milder, and E. Salman, "Error Probability Models for Voltage-Scaled Multiply-Accumulate Units," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 28, No. 7, pp. 1665-1675, July 2020
13. T. Wan, Y. Karimi, M. Stanacevic, and E. Salman, "AC Computing Methodology for RF-Powered IoT Devices," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 27, No. 5, pp. 1017-1028, May 2019
14. A. Ibrahim, M. Jain, E. Salman, R. Willing, and S. Towfighian, "A Smart Knee Implant Using Triboelectric Energy Harvesters," *Smart Materials and Structures*, Vol. 28, No. 2, Jan. 2019
15. W. Liu, C. Sitik, E. Salman, B. Taskin, S. Sundareswaran, and B. Huang, "SLECTS: Slew-Driven Clock Tree Synthesis," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 27, No. 4, pp. 864-874, April 2019
16. H. Liu, Y. Lu, J. Zhang, Y. Wang, and E. Salman, "Boosting the Efficiency of a Footstep Piezoelectric-Stack Energy Harvester by Using the Synchronized Switch Technology," *Journal of Intelligent Material Systems and Structures*, Vol. 30, No. 6, Feb. 2019
17. C. Yan, J. Dofe, S. Kontak, Q. Yu, and E. Salman, "Hardware-Efficient Logic Camouflaging for Monolithic 3D ICs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 65, No. 6, pp. 799-803, June 2018
18. C. Yan and E. Salman, "Mono3D: Open Source Cell Library for Monolithic 3D Integrated Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 65, No. 3, pp. 1075-1085, March 2018
19. C. Yan, Z. Gan, and E. Salman, "Package Embedded Spiral Inductor Characterization with Application to Switching Buck Converters," *Microelectronics Journal*, Vol. 66, pp. 41-47, August 2017
20. T. Wan, Y. Karimi, M. Stanacevic, and E. Salman, "Perspective Paper - Can AC Computing be an Alternative for Wirelessly Powered Devices?" *IEEE Embedded Systems Letters*, Vol. 9, No. 1, pp. 13-16, March 2017

21. H. Wang and E. Salman, "Closed-Form Expressions for I/O Simultaneous Switching Noise Revisited," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 2, pp. 769-773, February 2017

22. C. Sitik, W. Liu, B. Taskin, and E. Salman, "Design Methodology for Voltage-Scaled Clock Distribution Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 24, No. 10, pp. 3080-3093, October 2016

23. H. Wang and E. Salman, "Decoupling Capacitor Topologies for TSV-based 3D ICs with Power Gating," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 23, No. 12, pp. 2983-2991, December 2015

24. Z. Gan, E. Salman, and M. Stanacevic, "Figures-of-Merit to Evaluate the Significance of Switching Noise in Analog Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 23, No. 12, pp. 2945-2956, December 2015

25. C. Sitik, E. Salman, L. Filippini, S. J. Yoon, and B. Taskin, "FinFET-Based Low Swing Clocking," *ACM Journal on Emerging Technologies in Computing Systems*, Vol. 12, No. 2, pp. 13:1-13:20, August 2015

26. P. Ji and E. Salman, "Quantifying the Effect of Local Interconnects on On-Chip Power Distribution," *Microelectronics Journal*, Vol. 46, No. 3, pp. 258-264, March 2015

27. H. Wang, M. H. Asgari, and E. Salman, "Compact Model to Efficiently Characterize TSV-to-Transistor Noise Coupling in 3D ICs," *Integration, the VLSI Journal*, Vol. 47, No. 3, pp. 296-306, June 2014

28. S. M. Satheesh and E. Salman, "Power Distribution in TSV Based 3D Processor-Memory Stacks," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 2, No. 4, pp. 692-703, December 2012

29. E. Salman and E. G. Friedman, "Utilizing Interdependent Timing Constraints to Enhance Robustness in Synchronous Circuits," *Microelectronics Journal*, Vol. 43, No. 2, pp. 119-127, February 2012

30. S. Kose, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power/Ground Noise," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 8, pp. 1458-1468, August 2011

31. E. Salman and Q. Qi, "Path Specific Register Design to Reduce Standby Power Consumption," *Journal of Low Power Electronics and Applications*, Vol. 1, No. 1, pp. 131-149, April 2011

32. E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Methodology for Efficient Substrate Noise Analysis in Large Scale Mixed-Signal Circuits," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 10, pp. 1405-1418, October 2009

33. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Identification of Dominant Noise Source and Parameter Sensitivity for Substrate Coupling," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 10, pp. 1559-1564, October 2009

34. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Worst Case Power/Ground Noise Estimation Using an Equivalent Transition Time for Resonance," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, Vol. 56, No. 5, pp. 997-1004, May 2009

35. E. Salman, A. Dasdan, F. Taraporevala, K. Kucukcakar, and E. G. Friedman, "Exploiting Setup-Hold Time Interdependence In Static Timing Analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 6, pp. 1114-1125, June 2007

- **Refereed Conference Papers (IEEE/ACM)**

36. S. Alam and E. Salman, "Investigation of Single Event Transients on Monolithic 3D Integration Technology," *Hardened Electronics and Radiation Technology (HEART) Conference*, April 2025, to appear

37. A. Abdurrob, E. Salman, and J. Lombardi, "Energy-Efficient Co-Design for Octave Convolution in Deep Neural Networks Using ReRAM Crossbars," *Government Microcircuit Applications & Critical Technology Conference (GOMACTECH)*, March 2025, to appear

38. P. Shukla, M. Hajikhodaverdian, V. F. Pavlidis, E. Salman, and A. K. Coskun, "Energy-Efficient Dataflow Design for Monolithic 3D Systolic Arrays with Resistive RAM," *International Green and Sustainable Computing Conference*, November 2024 (received the best paper award)

39. O. Abdalla, E. Salman, M. Stanacevic, R. Willing, S. Towfighian, "Biocompatible Energy Harvester for Smart Knee Implants," *Smart Materials, Adaptive Structures and Intelligent Systems (SMASIS)*, October 2024

40. H. Haghshenas, E. Salman, R. Willing, S. Towfighian and M. Stanaćević, "A Triboelectric Nanogenerator Interface Circuit for Applied Force Sensing," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 428-432, August 2024

41. M. Pereira, A. Ahmad, Y. Xie, Y. Song, X. Sha, P. Djuric, M. Stanacevic, S. Das, E. Salman, and B. Glišic, "A novel passive embeddable RF sensor for structural health monitoring." *SPIE Sensors and Smart Structures Technologies for Civil, Mechanical, and Aerospace Systems*, vol. 12949, May 2024

42. K. Dhananjay, V. Pavlidis, A. K. Coskun, and E. Salman, "Enhanced Detection of Thermal Covert Channel Attacks in Multicore Processors," *IEEE International Symposium on Quality Electronic Design*, April 2024

43. H. Haghshenas, M. Chahari, E. Salman, R. Willing, S. Towfighian, and M. Stanacevic, "Power Transfer Optimization for Triboelectric Nanogenerators," *IEEE Biomedical Circuits and Systems Conference*, October 2023

44. A. Abdurrob, E. Salman, J. Lombardi, "Thermal Integrity of ReRAM-based Near-Memory Computing in 3D Integrated DNN Accelerators," *IEEE International System-on-Chip Conference*, September 2023

45. M. Rathore, P. Milder, and E. Salman, "Precision and Performance-Aware Voltage Scaling in DNN Accelerators," *ACM/IEEE Great Lakes Symposium on VLSI*, June 2023

46. I. Miketic, K. Dhananjay, and E. Salman, "Information-Theoretic Perspective to Thermal Covert Channels," *IEEE International Symposium on Circuits and Systems*, May 2023

47. M. Jain, M. Stanacevic, R. Willing, S. Towfighian, and E. Salman, "Wireless Power Transfer for Smart Knee Implants," *IEEE International Symposium on Circuits and Systems*, May 2022

48. K. Dhananjay and E. Salman, "EQUAL: Efficient QUasi Adiabatic Logic for Enhanced Side-Channel Resistance," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 332-337, July 2021

49. Z. Zhang, I. Miketic, E. Salman and Q. Yu, "Towards Enhancing Power-Analysis Attack Resilience for Logic Locking Techniques," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 132-137, July 2021

50. Z. Zhang, I. Miketic, E. Salman and Q. Yu, "Assessing Correlation Power Analysis (CPA) Attack Resilience of Transistor-Level Logic Locking," *ACM/IEEE Great Lakes Symposium on VLSI*, pp. 415-420, June 2021

51. P. Shukla, S. S. Nemtzow, V. Pavlidis, E. Salman, and A. Coskun, "Temperature-Aware Optimization of Monolithic 3D Deep Neural Network Accelerators," *IEEE/ACM Asia and South Pacific Design Automation Conference*, pp. 709-714, January 2021

52. K. Dhananjay and E. Salman, "Special Session: Adiabatic Circuits for Energy-Efficient and Secure IoT Systems," *IEEE International Conference on Computer Design*, October 2020

53. Y. Park and E. Salman, "High Efficiency Fully Integrated On-Chip Regulator for Wide-Range Output Current," *IEEE International Symposium on Circuits and Systems*, October 2020

54. I. Miketic and E. Salman, "Energy Efficient Adiabatic Circuits Using Transistor-Level Monolithic 3D Integration," *IEEE International System-on-Chip Conference*, September 2020

55. B. Gungor, M. Yazici, E. Salman, and Y. Gurbuz, "Establishing a Covert Communication Channel in RF and mm-Wave Circuits," *IEEE International Midwest Symposium on Circuits and Systems*, August 2020

56. M. Jain, N. A. Hossain, S. Towfighian, M. Stanacevic, and E. Salman, "System Prototype for a Triboelectric Harvester in a Smart Knee Implant," *SPIE Active and Passive Smart Structures and Integrated Systems IX*, April 2020

57. M. Jain, A. Ibrahim, E. Salman, M. Stanacevic, R. Willing, and S. Towfighian, "Frontend Electronic System for Triboelectric Harvester in a Smart Knee Implant," *IEEE International Midwest Symposium on Circuits and Systems*, August 2019

58. P. Shukla, A. Coskun, V. Pavlidis, and E. Salman, "An Overview of Thermal Challenges and Opportunities for Monolithic 3D ICs," *ACM/IEEE Great Lakes Symposium on VLSI*, pp. 439-444, May 2019

59. C. Sitik, W. Liu, B. Taskin, and E. Salman, "Low Voltage Clock Tree Synthesis with Local Gate Clusters," *ACM/IEEE Great Lakes Symposium on VLSI*, pp. 99-104, May 2019

60. I. Miketic and E. Salman, "Power and Data Integrity in Monolithic 3D Integrated SIMON Core," *IEEE International Symposium on Circuits and Systems*, May 2019

61. T. Noor and E. Salman, "A Novel Glitch-Free Integrated Clock Gating Cell for High Reliability," *IEEE International Symposium on Circuits and Systems*, May 2019

62. Y. Huang, T. Wan, E. Salman, and M. Stanacevic, "Signal Shaping at Interface of Wireless Power Harvesting and AC Computational Logic," *IEEE International Symposium on Circuits and Systems*, May 2019

63. M. Rathore, P. Milder, and E. Salman, "Towards TFET based Approximate Computing for Deep Learning," *Government Microcircuit Applications & Critical Technology Conference (GOMACTECH)*, pp. 340-345, March 2019

64. I. Miketic and E. Salman, "Monolithic 3D Integrated Encryption Core," *Government Microcircuit Applications & Critical Technology Conference (GOMACTECH)*, pp. 240-244, March 2019

65. A. Ibrahim, M. Jain, E. Salman, R. Willing, and S. Towfighian, "Feasibility of Triboelectric Energy Harvesting and Load Sensing in Total Knee Replacement," *The ASME Conference on Smart Materials, Adaptive Structures and Intelligent Systems*, September 2018

66. E. Salman, M. Stanacevic, S. Das, and P. Djuric, "Leveraging RF Power for Intelligent Tag Networks," *ACM/IEEE Great Lakes Symposium on VLSI*, pp. 329-334, May 2018

67. T. Wan and E. Salman, "Ultra Low Power SIMON Core for Lightweight Encryption," *IEEE International Symposium on Circuits and Systems*, May 2018

68. M. Rathore and E. Salman, "Error Probability Models for Low Voltage TFET Based Circuits," *IEEE International Symposium on Circuits and Systems*, May 2018

69. C. Yan and E. Salman, "Physical Design of Monolithic 3D ICs with Applications to Hardware Security," *Government Microcircuit Applications & Critical Technology Conference (GOMACTECH)*, pp. 702-707, March 2018

70. T. Wan, E. Salman, and M. Stanacevic, "AC Computing Methodology for RF Powered IoT Security," *Government Microcircuit Applications & Critical Technology Conference (GOMACTECH)*, pp. 939-944, March 2018

71. C. Yan and E. Salman, "Routing Congestion Aware Cell Library Development for Monolithic 3D ICs," *IEEE International Conference on Rebooting Computing*, November 2017

72. C. Yan, S. Kontak, H. Wang, and E. Salman, "Open Source Cell Library Mono3D to Develop Large-Scale Monolithic 3D Integrated Circuits," *IEEE International Symposium on Circuits and Systems*, pp. 2581-2584, May 2017

73. T. Wan, Y. Karimi, M. Stanacevic, and E. Salman, "Energy Efficient AC Computing Methodology for Wirelessly Powered IoT Devices," *IEEE Int. Symp. on Circuits and Systems*, pp. 509-512, May 2017

74. C. Yan, Z. Gan, and E. Salman, "In-Package Spiral Inductor Characterization for High Efficiency Buck Converters," *IEEE International Symposium on Circuits and Systems*, pp. 2396-2399, May 2017

75. J. Dofe, Z. Zhang, Q. Yu, C. Yan, and E. Salman, "Impact of Power Distribution Network on Power Analysis Attacks in Three-Dimensional Integrated Circuits," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 327-332, May 2017

76. J. Dofe, C. Yan, S. Kontak, E. Salman, and Q. Yu, "Transistor-Level Camouflaged Logic Locking Method for Monolithic 3D IC Security," *Proceedings of the IEEE Asian Hardware Oriented Security and Trust Symposium*, December 2016

77. J. Dofe, H. Wang, Q. Yu, and E. Salman, "Hardware Security Threats and Potential Countermeasures in Emerging 3D ICs," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 69-74, May 2016

78. T. Wan, E. Salman, and M. Stanacevic, "A New Circuit Design Framework for IoT Devices: Charge Recycling with Wireless Power Harvesting," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2046-2049, May 2016

79. Y. Park and E. Salman, "On-Chip Hybrid Regulator Topology for Portable SoCs with Near-Threshold Operation," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 786-789, May 2016

80. W. Liu, E. Salman, C. Sitik, and B. Taskin, "Exploiting Useful Skew in Gated Low Voltage Clock Trees for High Performance," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2595-2598, May 2016

81. L. Filippini, E. Salman, and B. Taskin, "A Wirelessly Powered System with Charge Recovery Logic," *Proceedings of the IEEE International Conference on Computer Design*, pp. 505-510, October 2015

82. W. Liu, E. Salman, C. Sitik, and B. Taskin, "Clock Skew Scheduling in the Presence of Heavily Gated Clock Networks," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 283-288, May 2015

83. M. Rathore, W. Liu, E. Salman, C. Sitik, and B. Taskin, "A Novel Static D Flip-Flop Topology for Low Swing Clocking," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 301-306, May 2015

84. S. Fang and E. Salman, "Low Swing TSV Signaling Using Novel Level Shifters with Single Supply Voltage," *Proceedings of the IEEE International Symp. on Circuits and Systems*, pp. 1965-1968, May 2015

85. W. Liu, E. Salman, C. Sitik, and B. Taskin, "Enhanced Level Shifter for Multi-Voltage Operation," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1442-1445, May 2015

86. H. Wang and E. Salman, "Resource Allocation Methodology for Through Silicon Vias and Sleep Transistors in 3D ICs," *Proc. of the IEEE International Symposium on Quality Electronic Design*, pp. 528-532, March 2015, **nominated for the best paper award**

87. H. Wang and E. Salman, "Enhancing System-Wide Power Integrity in 3D ICs with Power Gating," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 322-326, March 2015

88. C. Sitik, L. Filippini, E. Salman, and B. Taskin, "High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design," *Proc. of the IEEE Computer Society Annual Symposium on VLSI*, pp. 498-503, July 2014

89. H. Wang, M. H. Asgari, and E. Salman, "Efficient Characterization of TSV-to-Transistor Noise Coupling in 3D ICs," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 71-76, May 2013

90. S. M. Satheesh and E. Salman, "Effect of TSV Fabrication Technology on Power Distribution in 3D ICs," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 287-292, May 2013

91. H. Wang and E. Salman, "Power Gating Topologies in TSV Based 3D Integrated Circuits," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 327-328, May 2013

92. S. M. Satheesh and E. Salman, "Design Space Exploration for Robust Power Delivery in TSV Based 3D Systems-on-Chip," *Proceedings of the IEEE International System-on-Chip Conference*, pp. 307-311, September 2012

93. Z. Gan, E. Salman, and M. Stanacevic, "Methodology to Determine Dominant Noise Source in a System-on-Chip Based Implantable Device," *Proc. of the IEEE International System-on-Chip Conference*, pp. 115-119, September 2012

94. E. Salman, M. H. Asgari, and M. Stanacevic, "Signal Integrity Analysis of a 2D and 3D Integrated Potentiostat for Neurotransmitter Sensing," *Proc. of the IEEE Biomedical Circuits and Systems Conference*, pp.17-20, November 2011

95. E. Salman, "Noise Coupling Due to Through Silicon Vias (TSVs) in 3D Integrated Circuits," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1411-1414, May 2011

96. E. Salman, "Noise Management in Highly Heterogeneous SoC Based Integrated Circuits," *Proceedings of the IEEE International SoC Design Conference*, pp. 1-4, November 2010, **invited paper**

97. R. Secareanu, O. Hartin, J. Feddeler, R. Moseley, J. Shepherd, B. Vrignon, J. Yang, Q. Li, H. Zhao, W. Li, L. Wei, E. Salman, R. Wang, D. Blomberg, and P. Parris, "Impact of Low-Doped Substrate Areas on the Reliability of Circuits Subject to EFT Events," *Proceedings of the IEEE International SoC Design Conference*, pp. 21-24, November 2010

98. R. Jakushokas, E. Salman, E. G. Friedman, R. M. Secareanu, O. L. Hartin, and C. Recker, "Compact Substrate Models for Efficient Noise Coupling and Signal Isolation Analysis," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2346-2349, May/June 2010

99. E. Salman and E. G. Friedman, "Methodology to Achieve Higher Tolerance to Delay Variations in Synchronous Circuits," *Proceedings of the ACM/IEEE Great Lakes Symp. on VLSI*, pp. 447-452, May 2010

100. E. Salman and E. G. Friedman, "Reducing Delay Uncertainty in Deeply Scaled Integrated Circuits Using Interdependent Timing Constraints," *Proceedings of the ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, pp. 77-82, March 2010

101. Kose, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power Ground Noise," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2277-2280, May 2009

102. E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Contact Merging Algorithm for Efficient Substrate Noise Analysis in Large Scale Circuits," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 9-14, May 2009

103. S. Kose, E. Salman, Z. Ignjatovic, and E. G. Friedman, "Pseudo-Random Clocking to Enhance Signal Integrity," *Proceedings of the IEEE International System-on-Chip Conference*, pp. 47-50, September 2008

104. E. Salman and E. G. Friedman, "Methodology for Placing Localized Guard Rings to Reduce Substrate Noise in Mixed Signal Circuits," *Proc. of the 4th Conf. on PhD Research in Microelectronics and Electronics*, pp. 85-88, June 2008

105. E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Input Port Reduction for Efficient Substrate Extraction in Large Scale ICs," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 376-379, May 2008

106. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Equivalent Rise Time for Resonance in Power/Ground Noise Estimation," *Proc. of the IEEE International Symposium on Circuits and Systems*, pp. 2422-2425, May 2008

107. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Dominant Substrate Noise Coupling Mechanism for Multiple Switching Gates," *Proc. of the IEEE Int. Symposium on Quality Electronic Design*, pp. 261-266, March 2008

108. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Substrate Noise Reduction Based On Noise Aware Cell Design," *Proc. of the IEEE International Symposium on Circuits and Systems*, pp. 3227-3230, May 2007, **invited paper**

109. E. Salman, E. G. Friedman, and R. M. Secareanu, "Substrate and Ground Noise Interactions in Mixed-Signal Circuits," *Proceedings of the IEEE International System-on-Chip Conference*, pp. 293-296, September 2006

110. E. Salman, A. Dasdan, F. Taraporevala, K. Kucukcakar, and E. G. Friedman, "Pessimism Reduction in Static Timing Analysis Using Interdependent Setup and Hold Times," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 159-164, March 2006, **nominated for the best paper award**

111. E. Salman, H. Akin, O. Gursoy, A. Ergintav, I. Tekin, A. Bozkurt, and Y. Gurbuz, "Design of a 3.2 mW PLL Based Clock and Data Recovery Circuit in 90-nm CMOS Technology," *Proceedings of the Mediterranean Microwave Symposium*, September 2005

- **Nonrefereed Publications and Reports**

112. W. Liu, C. Sitik, E. Salman, B. Taskin, S. Sundareswaran, and B. Huang, "Slew-Driven Clock Tree Synthesis (SLECTS) Methodology to Facilitate Low Voltage Clocking," *Semiconductor Research Corporation (SRC) Technology Conference (TECHCON)*, September 2016

113. T. Wan, Y. Karimi, E. Salman, and M. Stanacevic, "A New Circuit Design Framework for IoT Devices," *International Conference and Expo on Emerging Technologies for a Smarter World*, October 2015

114. W. Liu, E. Salman, C. Sitik, B. Taskin, S. Sundareswaran, and B. Huang, "Circuits and Algorithms to Facilitate Low Swing Clocking in Nanoscale Technologies," *Semiconductor Research Corporation (SRC) Technology Conference (TECHCON)*, September 2015

115. E. Salman and M. Stanacevic, "3-D Integrated Implantable Device for Deep Brain Sensing and Stimulation," *International Conference and Expo on Emerging Technologies for a Smarter World*, November 2011

116. G. Bischof, B. Scholnick, and E. Salman, "Fully Integrated PLL Based Clock Generator for Implantable Biomedical Applications," *IEEE Annual Conference on Long Island Systems, Applications and Technology*, May 2011

117. E. Salman, A. Doboli, and M. Stanacevic, "Noise and Interference Management in 3-D Integrated Wireless Systems," *International Conference and Expo on Emerging Technologies for a Smarter World*, September 2010

Professional Activities

- **Memberships**
  - Chair, VLSI Systems and Applications Technical Committee (VSA-TC), IEEE Circuits and Systems Society, 2020 to 2022
  - Chair-Elect, VLSI Systems and Applications Technical Committee (VSA-TC), IEEE Circuits and Systems Society, 2018 to 2020
  - Senior Member, IEEE, 2017 to present
  - Member, IEEE, 2003 to 2017
  - Member, IEEE Circuits and Systems Society, 2013 to present

- Technical committee member, VLSI Systems and Applications Technical Committee (VSA-TC), IEEE Circuits and Systems Society, 2015 to present

- **Editorial Activities**
  - Associate Editor, IEEE Transactions on Emerging Topics in Computing, 2020 to present
  - Regional editor, Journal of Circuits, Systems and Computer, July 2013 to present
    - One of the five managing editors of the journal
  - Guest Editor, IEEE Trans. on Circuits and Systems - I: Regular Papers, 2019
  - Guest Editor, IEEE Trans. on Circuits and Systems - II: Express Briefs, 2019
  - Associate editor, Journal of Low Power Electronics and Applications, 2010 to present
  - Associate editor, IEEE Trans. on Very Large Scale Integration (VLSI) Systems, 2011 to 2015
- **Selected Conference and Organizational Activities**
  - Computer-Aided Design Track Chair, ACM/IEEE Great Lakes Symp. on VLSI, 2021 and 2022
  - Digital Integrated Circuits Track Chair, IEEE International Symposium on Circuits and Systems, 2018 to 2022
  - VLSI Track Chair, IEEE International Midwest Symp. on Circuits and Systems, 2018 and 2020
  - Special Sessions Chair, ACM/IEEE Great Lakes Symposium on VLSI, 2017
  - Finance Chair, ACM/IEEE System Level Interconnect Prediction, 2016
  - Registration Chair, ACM/IEEE Great Lakes Symposium on VLSI, 2016
  - Publicity chair, ACM Design Automation Conference PhD Forum, 2012
- **Selected Technical Program Committees**
  - ACM/IEEE Design Automation Conference, 2022
  - IEEE International Conference on Computer Design, 2020 to present
  - ACM/IEEE Great Lakes Symposium on VLSI, 2013 to present
  - IEEE International Symposium on Quality Electronic Design, 2015 to present
  - ACM/IEEE System Level Interconnect Prediction, 2016 to 2019
  - IEEE Conference on Electron Devices and Solid-State Circuits, 2015 and 2016
- **Organized Special Sessions**
  - Revisiting Adiabatic Circuits in the Era of Energy-Efficiency and Security, International Conference on Computer Design, 2020
  - Opportunities and Challenges for Emerging Monolithic 3D Integrated Circuits, ACM/IEEE Great Lakes Symposium on VLSI, 2019
  - Circuits and Systems for Autonomous IoT Devices, ACM/IEEE Great Lakes Symposium on VLSI, 2018
  - Energy-Efficient and Secure IoT, IEEE Int. Symposium on Circuits and Systems, 2017
  - Circuit and System Design for Emerging IoT Applications, IEEE Int. Symposium on Circuits and Systems, 2016

Teaching Activity

- ESE 555 Advanced VLSI Systems Design
  - Project-based graduate VLSI course with emphasis on delay/timing and power analysis, low power design techniques, combinational and sequential circuits, and design of data paths
- ESE 585 Nanoscale Integrated Circuit Design
  - Advanced VLSI graduate course with emphasis on interconnect-centric IC design process such global signaling methodologies, power delivery, and clock distribution networks
- ESE 324 Advanced Electronics Laboratory
  - Experimental undergraduate lab course with emphasis on building and testing digital, analog, and mixed-signal circuits such as frequency dividers, oscillators, phase-locked loops, data converters, and DC-DC voltage converters
- ITS/SBU 102 Introduction to Modern Chip Design
  - Seminar course open to university-wide freshmen population, with emphasis on the important issues at the intersection of engineering and chip design process, distributed semiconductor supply chain, potential ethical issues related to microelectronics, and contribution of microelectronic chips to climate change

Service and Outreach

- **Departmental Service**
  - Industry Liaison, 2016-present
    - Coordinating the Department's relationships with the corporate world
  - Supervisor for J. Joseph, System and Network Administrator, 2018-present
  - Graduate Committee Member, 2016-present
  - Search Committee Chair for Instructional Support Technician, 2021
  - Faculty Search Committee Chair for two senior-level Empire Innovation Professor faculty positions in power electronics and power/energy systems, 2019
  - Electrical Engineering Curriculum Review Committee Member, 2017-2018
  - Hiring Committee Member for Professor in Practice, 2018
  - ECE Chair Search Committee Member, 2016
  - Undergraduate Committee Member, 2011 to 2016
  - Graduate Admissions Committee Member, 2011 to 2015
  - Committee Member for PhD Qualifying Exam in VLSI and Circuits, 2011-2017
  - ABET Assessment Committee Chair for ESE 324, 2011 to present
  - Member of Various PhD Dissertation Defense Committees, 2010-present
  - Panelist at Graduate School Discussion for ECE Honors Students, 2013
  - Panelist at ECE Honors Seminar on Theory versus Experiment, 2015
- **College Service**
  - Personnel Policy Committee (PPC) Member for CEAS, Spring 2024-present
  - SBU 102 Seminar Instructor, Spring 2023
  - Reviewer of research proposals for the SUNY-IBM Alliance, Spring 2022
  - Information and Technology Studies (ITS) 102 Instructor, Spring 2015
  - Information and Technology Studies (ITS) Round Table: Chat with Professors, 2012-2018
  - Panelist at the New Teaching Assistant Orientation, 2011

- **University Service**
  - Member of a Tiger Team (organized by Provost and Office of Vice President for Research) focusing on High-Performance Computing, Semiconductors, Advanced Computer Hardware/Software, 2021-2022
  - Reviewer for OVPR Seed Grant Program, 2019-present
  - Reviewer for URECA Summer Research Fellowship Program, 2020
  - Platform Party Marshall, 59^{th} Commencement, Stony Brook University, 2019

Graduate Students

- **Current PhD Students**
  - Abrar Abdurrob, expected May 2025
  - Nicholas St. John (part time PhD student), expected May 2026
  - Sakila Alam, expected May 2026
  - Maryam Hosseini, expected May 2027
  - Hanchen Li, expected May 2027
- **Current MSc Students with Thesis**
  - Suvarna Tirur Ananthanarayan, expected May 2024
- **PhD Alumni**
  - Dr. Ivan Miketic, August 2023
    - First position: Apple Inc., Cupertino, CA
    - Dissertation: Hardware Security Techniques against Information Leakage and Counterfeiting in Integrated Circuits
  - Dr. Krithika Dhananjay, June 2022
    - First position: Qualcomm, MA
    - Dissertation: Detecting and Mitigating Hardware Security Attacks in Emerging Technologies and Applications
  - Dr. Mallika Rathore, May 2021
    - First position: Google, Sunnyvale, CA
    - Dissertation: Exploring the Accuracy vs. Energy Efficiency Trade-offs in Error-Aware Low Voltage DNN Accelerators
  - Dr. Manav Jain, May 2021
    - First position: Intel Corp., San Jose, CA
    - Dissertation: Frontend Electronic System for a Triboelectric Harvester in a Smart Knee Implant
  - Dr. Tutu Wan, December 2019
    - First position: Apple Inc., Cupertino, CA
    - Dissertation: AC Computing Methodology for Wirelessly Powered Devices
  - Dr. Chen Yan, December 2018
    - First position: GlobalFoundries, Albany, NY
    - Dissertation: Leveraging Monolithic 3D Integrated Circuit Technology for Emerging Applications
  - Dr. Weicheng Liu, January 2018
    - First position: NXP Semiconductors, Austin, TX
    - Dissertation: Low Voltage Clocking Methodologies for Nanoscale ICs

- Dr. Zhihua Gan, August 2017
  - First position: Nordco, Beacon Falls, CT
  - Dissertation: Design Methodologies to Manage Switching Noise with Applications to Biomedical Acoustic Systems
- Dr. Hailang Wang, January 2016
  - First position: Apple Inc., Cupertino, CA
  - Dissertation: Enhancing Power and Signal Integrity in Three-Dimensional Integrated Circuits

- **MSc Alumni with Thesis**
  - Bryan Moy, December 2020
    - First position: Apple Inc., Cupertino, CA
    - Thesis: Lightweight Encryption for Resource Constrained Systems
  - Yongwan Park, May 2016
    - First position: Ph.D. student at University of Maryland College Park
    - Thesis: Fully Integrated Hybrid Voltage Regulator for Low Voltage Applications
  - Sushil Panda, May 2016
    - First position: Dolphin Technology, Santa Clara, CA
    - Thesis: Investigating the Tolerance of Wirelessly Powered Charge-Recycling Logic to Power-Clock Phase Difference Deviations
  - Tasnuva Noor, May 2016
    - First position: Brookhaven National Laboratory, Brookhaven, NY
    - Thesis: Design of a Novel Glitch-Free Integrated Clock Gating Cell for High Reliability
  - Mallika Rathore, May 2014
    - First position: Marvell Semiconductor, Boise, ID
    - Thesis: Design and Analysis of Custom Clock Buffers and a D Flip-Flop for Low Swing Clock Distribution Networks
  - Peirong Ji, December 2013
    - First position: SK Hynix, San Jose, CA
    - Thesis: Quantifying the Effect of Local Power Distribution Network and Vias on Power Integrity
  - Sateja Mungi, May 2013
    - First position: Intel Corporation, Hudson, MA
    - Thesis: Effective Distance Calculations for On-Chip Decoupling Capacitors in 3D ICs
  - Ziqi Zhang, May 2013
    - First position: Marvell Semiconductor, San Jose, CA
    - Thesis: Comparative Analysis of Near-Threshold and Charge Recovery Circuits for Energy Efficiency and Performance
  - Ajay Chandrasekhar, May 2013
    - First position: Imagination Technologies, San Jose, CA
    - Thesis: Critical Length Estimation for TSV-Based 3D Sub/Near-Threshold Circuits
  - Suhas M. Satheesh, May 2012
    - First position: NVIDIA, Santa Clara, CA
    - Thesis: Power Distribution in TSV Based 3D Processor-Memory Stacks
  - Mohammad H. Asgari, December 2011
    - First position: Ph.D. student at Columbia University, New York, NY

    - Thesis: TSV Related Noise Coupling in 3D Integrated Circuits

- **Undergraduate Research and Advising**
  - Isac Park, 2022-2023
    - Senior design project
  - William Ji, 2022-2023
    - Senior design project
  - Chuming Tang, 2022-2023
    - Senior design project
  - Alexander Ahandour, 2019-2020 (co-advised with Prof. Peter Milder)
    - Senior design project
    - ECE Honors Research
  - Zhen Sin (William) Wong, 2019-2020 (co-advised with Prof. Peter Milder)
    - Senior design project
  - Sabreen Mostafa, 2019-2020 (co-advised with Prof. Peter Milder)
    - Senior design project
  - Mariano Bello, 2019-2020 (co-advised with Prof. Peter Milder)
    - Senior design project
  - Nicholas St. John, 2018-2019
    - Senior design project
    - First position: Engineer at Brookhaven National Labs, NY
  - Bryan Moy, 2018-2019
    - Senior design project
    - First position: Hardware Engineer at Apple, Cupertino, CA
  - William Lee, 2018-2019
    - Senior design project
  - Seongmin Han, 2016-2017
    - Senior design project
  - Scott Kontak, 2016-2017
    - NSF REU scholarship
    - Co-author of several IEEE/ACM papers
    - First position: Ph.D. student at Columbia University, NY
  - Xiaoxi Zhang, 2016-2017
    - ECE Honors research
    - First position: Signal Integrity Engineer at Intel, Hillsboro, OR
  - Joram Mercado, 2015-2017
    - Senior design project
    - Independent research
    - First position: M.Sc. student at Stony Brook University
  - Jea Won Kwon, 2015-2016
    - Senior design project
  - Yongwan Park, 2014-2015
    - NSF REU scholarship

    - Senior design project
    - First author of an IEEE ISCAS 2016 paper
    - First position: M.Sc. student at Stony Brook University, Ph.D. student at University of Maryland
- Shiwei Fang, 2013-2014
    - ECE honors research
    - First author of an IEEE ISCAS 2015 paper
    - Recipient of Provost Award for Academic Excellence
    - Recipient of Undergraduate Recognition Award
    - First position: Ph.D. student at University of North Carolina at Chapel Hill
- Sung Jun Yoon, 2012-2013
    - URECA (Undergraduate Research and Creative Activities) fellowship
    - Co-author of an ACM journal paper
    - First position: Ph.D. student at Texas A&M University
- Jongmun Hwang, 2012-2013
    - Senior design project
- Artem Ayzen, 2011-2012
    - Senior design project
- Garrett Bischof, 2010-2011
    - Senior design project
    - First author of a LISAT 2011 paper
- Ben Scholnick, 2010-2011
    - Senior design project
    - Co-author of a LISAT 2011 paper