Emre Salman

Contact Information

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Electrical and Computer Engineering
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Research Interests

- Nanoscale integrated circuits and systems with application to
  - Energy-efficient and secure computing
  - Internet-of-things with energy harvesting
  - Implantable bio-electronics
- Emerging integrated circuit and system technologies

Education

University of Rochester, Rochester, New York USA

Ph.D., Electrical Engineering, May 2009

- Advisor: Eby G. Friedman

M.S., Electrical and Computer Engineering, May 2006

Sabanci University, Istanbul, Turkey

B.S., Microelectronics Engineering, July 2004

Professional Experience

Stony Brook University (SUNY), Stony Brook, New York USA

Associate Professor — **September, 2016 - present**
Electrical and Computer Engineering

Director — **September, 2011 - present**
Nanoscale Circuits and Sysems (NanoCAS) Laboratory

Assistant Professor — **September, 2010 - August, 2016**
Electrical and Computer Engineering

University of Rochester, Rochester, New York USA

Post-doctoral Research Associate — **June, 2009 - August, 2010**
Electrical and Computer Engineering

Instructor — **January, 2010 - July, 2010**
Rochester Scholars Program

Research Assistant — **September, 2005 - May, 2009**
Electrical and Computer Engineering

Freescale Semiconductor, Tempe, Arizona USA

Research Intern — **Summer 2006 and 2007**
Microwave and Mixed-Signal Technologies

Synopsys, Mountain View, California USA

Research Intern **Summer 2005**
PrimeTime Group

STMicroelectronics, Istanbul, Turkey

IC Design Engineer **September, 2003 - June, 2004**
Analog and Mixed-Signal Team

Honors and Awards

- Stony Brook University Inaugural Leadership Academy Fellow, Spring 2017
  - Selected every year from a pool of associate professors nominated by departmental chairs. The fellows participate in various leadership workshops.
- Invited Paper, IEEE Transactions on Circuits and Systems - I: Regular Papers, June 2017
  - C. Yan and E. Salman, "Mono3D: Open Source Cell Library for Monolithic 3D Integrated Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, in press
- Best Paper Award, Semiconductor Research Corporation (SRC) TECHCON, September 2016
  - W. Liu, C. Sitik, E. Salman, B. Taskin, S. Sundareswaran, and B. Huang, "Slew-Driven Clock Tree Synthesis Methodology to Facilitate Low Voltage Clocking," *SRC Technology Conference (TECHCON)*, September 2016
  - "TECHCON is SRC's premiere event, showcasing both the best member-sponsored research, and the top student-researchers."
- Best Paper Nomination, IEEE Int. Symp. on Quality Electronic Design, March 2015
  - H. Wang and E. Salman, "Resource Allocation Methodology for Through Silicon Vias and Sleep Transistors in 3D ICs," *Proc. of the IEEE International Symposium on Quality Electronic Design*, pp. 528-532, March 2015
  - One of the 8 papers nominated for the best paper award out of 125 accepted papers
- Stony Brook University Inaugural Discovery Fund Prize Finalist, December 2014
  - For research on leveraging AC computing for wirelessly powered devices
  - "The Discovery Fund is Stony Brook University's response to a nationwide call to augment public funding of university research with philanthropic support with emphasis on high risk, high reward research addressing modern problems."
- IEEE Long Island Outstanding Young Engineer Award, March 2014
  - For contributions to developing robust and heterogeneous 3D integrated circuits
  - "This award honors a Long Island IEEE member who has made important technical contributions prior to his or her 35^{th} birthday."
- National Science Foundation (NSF) CAREER Award, March 2013
  - For research on "leveraging 3D integration technology for highly heterogeneous SoCs"
- IEEE Circuits and Systems Society, Outreach Initiative Award, 2012, 2013, 2015, 2017
  - For organizing high impact outreach activities in Long Island, New York
- Invited Paper, IEEE Transactions on Circuits and Systems - I: Regular Papers, January 2009
  - E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Worst Case Power/Ground Noise Estimation Using an Equivalent Transition Time for Resonance," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, Vol. 56, No. 5, pp. 997-1004, May 2009

- Best Paper Nomination, IEEE Int. Symp. on Quality Electronic Design, March 2006
  - E. Salman, A. Dasdan, F. Taraporevala, K. Kucukcakar, and E. G. Friedman, "Pessimism Reduction in Static Timing Analysis Using Interdependent Setup and Hold Times," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 159-164, March 2006

Selected Media Coverage

- Wireless Energy Harvesting for IoT Devices
  - `https://sciencenode.org/feature/wireless-energy-harvesting-for-iot-devices.php`
- Stony Brook Discovery Fund Challenge Held at Simons Foundation
  - `https://www.simonsfoundation.org/features/foundation-news/stony-brook-discovery-fund-challenge-held-at-simons-foundation/`
- Stony Brook Announces Four Finalists for Inaugural Discovery Fund Award
  - `http://www.labmanager.com/news/2014/11/stony-brook-announces-four-finalists-for-inaugural-discovery-fund-award`
- Scientist developing 3-D chips to expand capacity of microprocessors
  - `http://www.nsf.gov/mobile/discoveries/disc_summ.jsp?cntn_id=130314&org=NSF`
- Smaller, better, faster, stronger 3D chips
  - `https://sciencenode.org/spotlight/smaller-better-faster-stronger-3d-chips.php`
- New Research Advances Heterogeneous 3D Chip Design
  - `http://www.hpcwire.com/2014/02/06/researcher-advances-heterogenous-3d-chip-design/`
- Our graduate receives half a million in funding
  - `http://gazetesu.sabanciuniv.edu/en/2014-01/our-graduate-receives-half-million-funding`

Grants and Contracts

1. National Science Foundation (NSF), "SaTC: STARSS: Small: Collaborative: Managing Hardware Security in Three-Dimensional Integrated Circuits," $220,000, **Sole PI** at Stony Brook, 10/2017-9/2020 (NSF and SRC joint funding).

2. National Institute of Health (NIH), "An Implantable Self-Powered Load Sensor for Total Knee Replacement Health Monitoring," $112,824, **Sole PI** at Stony Brook, 9/2017-8/2019, sub-contract from Binghamton University

3. National Science Foundation (NSF), "CPS: Breakthrough: Charge-Recycling based Computing Paradigm for Wirelessly Powered Internet-of-Things," $425,000, PI/PD, 9/2016-8/2019 (with M. Stanacevic, received 50%)

4. Simons Foundation, "New Milestone in Energy Autonomy: Novel Charge-Recycling Circuits for Wireless Power Harvesting," $50,000 (gift), PI/PD, 11/2014-12/2017

5. Semiconductor Research Corporation (SRC), "Design and Automation of a Novel Low Swing Clocking Methodology with Reduced Delay Uncertainty," $225,000, PI/PD, 10/2013-3/2017 (with B. Taskin, received 50%)

6. Office of the Vice President for Research (OVPR) at Stony Brook University, "CAREER: Leveraging Three-Dimensional Integration Technology for Highly Heterogeneous Systems-on-Chip," $35,000, sole PI, 7/2013-6/2015

7. National Science Foundation (NSF), "CAREER: Leveraging Three-Dimensional Integration Technology for Highly Heterogeneous Systems-on-Chip," $453,809, sole PI, 3/2013-2/2018
8. IEEE Circuits and Systems Society, "Outreach Activities for High School Students: Educating Electrical Engineers of the Future," $21,300, PI/PD, 10/2012-9/2016

Publications

- **Book**

1. E. Salman and E. G. Friedman, *High Performance Integrated Circuit Design*, McGraw-Hill, ISBN:0071635769, September 2012
   - Comprehensive tutorial book (716 pages) that unifies interconnect-centric design methodologies in nanoscale ICs, representing a new generation of textbooks
   - Adopted as a textbook for graduate level courses at multiple higher education institutions
   - Translated into Chinese by Electronic Industry Press, ISBN 7121250903, January 2015

- **Patents**

1. E. Salman, M. Stanacevic, T. Wan, and Y. Karimi, "Radio Frequency (RF) Energy Harvesting and Method for Utilizing the Same," US Patent Pending
2. B. Taskin, C. Sitik, E. Salman, and W. Liu, "Slew-Aware Clock Tree Synthesis," US Patent pending
3. A. Dasdan, E. Salman, F. Taraporevala, and K. Kucukcakar, "Characterizing Sequential Cells Using Interdependent Setup and Hold Times, and Utilizing the Sequential Cell Characterization in Static Timing Analysis," US Patent No 7,506,293
4. R. M. Secareanu, O. L. Hartin, and E. Salman, "Apparatus and Method For Reducing Noise in Mixed-Signal Circuits and Digital Circuits," US Patent No 7,834,428

- **Invited Book Chapters**

1. E. Salman, "On-Chip Regulators for Low Voltage and Portable Systems-on-Chip," *Energy Efficient Technologies: Devices, Circuits, and Systems*, S. Kurinec and K. Iniewski (Eds.), CRC Press, to appear
2. E. Salman, "Substrate Induced Signal Integrity in 2D and 3D ICs," *Noise Coupling in System-on-Chip*, pp. 21-44, T. Noulis (Ed.), CRC Press, December 2017
3. E. Salman, "Power and Signal Integrity Challenges in 3D Systems-on-Chip," *Physical Design for 3D Integrated Circuits*, pp. 101-126, A. Todri-Sanial and C. S. Tan (Eds.), CRC Press, December 2015
4. M. Stanacevic, Y. Lin, and E. Salman, "Analysis and Design of 3D Potentiostat for Deep Brain Implantable Devices," *Neural Computation, Neural Devices, and Neural Prosthesis*, pp. 261-287, Z. Yang (Ed.), Springer, 2014

- **Journal Papers**

1. C. Yan and E. Salman, "Mono3D: Open Source Cell Library for Monolithic 3D Integrated Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, to appear
2. C. Yan, J. Dofe, S. Kontak, Q. Yu, and E. Salman, "Hardware-Efficient Logic Camouflaging for Monolithic 3D ICs," *IEEE Transactions on Circuits and Systems II: Express Briefs*, to appear
3. C. Yan, Z. Gan, and E. Salman, "Package Embedded Spiral Inductor Characterization with Application to Switching Buck Converters," *Microelectronics Journal*, Vol. 66, pp. 41-47, August 2017
4. T. Wan, Y. Karimi, M. Stanacevic, and E. Salman, "Perspective Paper - Can AC Computing be an Alternative for Wirelessly Powered Devices?" *IEEE Embedded Systems Letters*, Vol. 9, No. 1, pp. 13-16, March 2017

5. H. Wang and E. Salman, "Closed-Form Expressions for I/O Simultaneous Switching Noise Revisited," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 2, pp. 769-773, February 2017

6. C. Sitik, W. Liu, B. Taskin, and E. Salman, "Design Methodology for Voltage-Scaled Clock Distribution Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 24, No. 10, pp. 3080-3093, October 2016

7. H. Wang and E. Salman, "Decoupling Capacitor Topologies for TSV-based 3D ICs with Power Gating," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 23, No. 12, pp. 2983-2991, December 2015

8. Z. Gan, E. Salman, and M. Stanacevic, "Figures-of-Merit to Evaluate the Significance of Switching Noise in Analog Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 23, No. 12, pp. 2945-2956, December 2015

9. C. Sitik, E. Salman, L. Filippini, S. J. Yoon, and B. Taskin, "FinFET-Based Low Swing Clocking," *ACM Journal on Emerging Technologies in Computing Systems*, Vol. 12, No. 2, pp. 13:1-13:20, August 2015

10. P. Ji and E. Salman, "Quantifying the Effect of Local Interconnects on On-Chip Power Distribution," *Microelectronics Journal*, Vol. 46, No. 3, pp. 258-264, March 2015

11. H. Wang, M. H. Asgari, and E. Salman, "Compact Model to Efficiently Characterize TSV-to-Transistor Noise Coupling in 3D ICs," *Integration, the VLSI Journal*, Vol. 47, No. 3, pp. 296-306, June 2014

12. S. M. Satheesh and E. Salman, "Power Distribution in TSV Based 3D Processor-Memory Stacks," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 2, No. 4, pp. 692-703, December 2012

13. E. Salman and E. G. Friedman, "Utilizing Interdependent Timing Constraints to Enhance Robustness in Synchronous Circuits," *Microelectronics Journal*, Vol. 43, No. 2, pp. 119-127, February 2012

14. S. Kose, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power/Ground Noise," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 8, pp. 1458-1468, August 2011

15. E. Salman and Q. Qi, "Path Specific Register Design to Reduce Standby Power Consumption," *Journal of Low Power Electronics and Applications*, Vol. 1, No. 1, pp. 131-149, April 2011

16. E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Methodology for Efficient Substrate Noise Analysis in Large Scale Mixed-Signal Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 10, pp. 1405-1418, October 2009

17. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Identification of Dominant Noise Source and Parameter Sensitivity for Substrate Coupling," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 10, pp. 1559-1564, October 2009

18. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Worst Case Power/Ground Noise Estimation Using an Equivalent Transition Time for Resonance," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, Vol. 56, No. 5, pp. 997-1004, May 2009

19. E. Salman, A. Dasdan, F. Taraporevala, K. Kucukcakar, and E. G. Friedman, "Exploiting Setup-Hold Time Interdependence In Static Timing Analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 6, pp. 1114-1125, June 2007

- **Refereed Conference Papers (IEEE/ACM)**

20. C. Yan and E. Salman, "Characterization and Physical Design of Large Scale Monolithic 3D Integrated Circuits," *Government Microcircuit Applications & Critical Technology Conference*, March 2018, to appear

21. T. Wan, E. Salman, and M. Stanacevic, "AC Computing Methodology for RF Power Harvesting," *Government Microcircuit Applications & Critical Technology Conference*, March 2018, to appear

22. C. Yan and E. Salman, "Routing Congestion Aware Cell Library Development for Monolithic 3D ICs," *IEEE International Conference on Rebooting Computing*, November 2017

23. C. Yan, S. Kontak, H. Wang, and E. Salman, "Open Source Cell Library Mono3D to Develop Large-Scale Monolithic 3D Integrated Circuits," *IEEE International Symposium on Circuits and Systems*, pp. 2581-2584, May 2017

24. T. Wan, Y. Karimi, M. Stanacevic, and E. Salman, "Energy Efficient AC Computing Methodology for Wirelessly Powered IoT Devices," *IEEE Int. Symp. on Circuits and Systems*, pp. 509-512, May 2017

25. C. Yan, Z. Gan, and E. Salman, "In-Package Spiral Inductor Characterization for High Efficiency Buck Converters," *IEEE International Symposium on Circuits and Systems*, pp. 2396-2399, May 2017

26. J. Dofe, Z. Zhang, Q. Yu, C. Yan, and E. Salman, "Impact of Power Distribution Network on Power Analysis Attacks in Three-Dimensional Integrated Circuits," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 327-332, May 2017

27. J. Dofe, C. Yan, S. Kontak, E. Salman, and Q. Yu, "Transistor-Level Camouflaged Logic Locking Method for Monolithic 3D IC Security," *Proceedings of the IEEE Asian Hardware Oriented Security and Trust Symposium*, December 2016

28. J. Dofe, H. Wang, Q. Yu, and E. Salman, "Hardware Security Threats and Potential Countermeasures in Emerging 3D ICs," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 69-74, May 2016

29. T. Wan, E. Salman, and M. Stanacevic, "A New Circuit Design Framework for IoT Devices: Charge Recycling with Wireless Power Harvesting," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2046-2049, May 2016

30. Y. Park and E. Salman, "On-Chip Hybrid Regulator Topology for Portable SoCs with Near-Threshold Operation," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 786-789, May 2016

31. W. Liu, E. Salman, C. Sitik, and B. Taskin, "Exploiting Useful Skew in Gated Low Voltage Clock Trees for High Performance," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2595-2598, May 2016

32. L. Filippini, E. Salman, and B. Taskin, "A Wirelessly Powered System with Charge Recovery Logic," *Proceedings of the IEEE International Conference on Computer Design*, pp. 505-510, October 2015

33. W. Liu, E. Salman, C. Sitik, and B. Taskin, "Clock Skew Scheduling in the Presence of Heavily Gated Clock Networks," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 283-288, May 2015

34. M. Rathore, W. Liu, E. Salman, C. Sitik, and B. Taskin, "A Novel Static D Flip-Flop Topology for Low Swing Clocking," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 301-306, May 2015

35. S. Fang and E. Salman, "Low Swing TSV Signaling Using Novel Level Shifters with Single Supply Voltage," *Proceedings of the IEEE International Symp. on Circuits and Systems*, pp. 1965-1968, May 2015

36. W. Liu, E. Salman, C. Sitik, and B. Taskin, "Enhanced Level Shifter for Multi-Voltage Operation," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1442-1445, May 2015

37. H. Wang and E. Salman, "Resource Allocation Methodology for Through Silicon Vias and Sleep Transistors in 3D ICs," *Proc. of the IEEE International Symposium on Quality Electronic Design*, pp. 528-532, March 2015, **nominated for the best paper award**

38. H. Wang and E. Salman, "Enhancing System-Wide Power Integrity in 3D ICs with Power Gating," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 322-326, March 2015

39. C. Sitik, L. Filippini, E. Salman, and B. Taskin, "High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design," *Proc. of the IEEE Computer Society Annual Symposium on VLSI*, pp. 498-503, July 2014

40. H. Wang, M. H. Asgari, and E. Salman, "Efficient Characterization of TSV-to-Transistor Noise Coupling in 3D ICs," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 71-76, May 2013

41. S. M. Satheesh and E. Salman, "Effect of TSV Fabrication Technology on Power Distribution in 3D ICs," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 287-292, May 2013

42. H. Wang and E. Salman, "Power Gating Topologies in TSV Based 3D Integrated Circuits," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 327-328, May 2013

43. S. M. Satheesh and E. Salman, "Design Space Exploration for Robust Power Delivery in TSV Based 3D Systems-on-Chip," *Proceedings of the IEEE International System-on-Chip Conference*, pp. 307-311, September 2012

44. Z. Gan, E. Salman, and M. Stanacevic, "Methodology to Determine Dominant Noise Source in a System-on-Chip Based Implantable Device," *Proc. of the IEEE International System-on-Chip Conference*, pp. 115-119, September 2012

45. E. Salman, M. H. Asgari, and M. Stanacevic, "Signal Integrity Analysis of a 2D and 3D Integrated Potentiostat for Neurotransmitter Sensing," *Proc. of the IEEE Biomedical Circuits and Systems Conference*, pp.17-20, November 2011

46. E. Salman, "Noise Coupling Due to Through Silicon Vias (TSVs) in 3D Integrated Circuits," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1411-1414, May 2011

47. E. Salman, "Noise Management in Highly Heterogeneous SoC Based Integrated Circuits," *Proceedings of the IEEE International SoC Design Conference*, pp. 1-4, November 2010, **invited paper**

48. R. Secareanu, O. Hartin, J. Feddeler, R. Moseley, J. Shepherd, B. Vrignon, J. Yang, Q. Li, H. Zhao, W. Li, L. Wei, E. Salman, R. Wang, D. Blomberg, and P. Parris, "Impact of Low-Doped Substrate Areas on the Reliability of Circuits Subject to EFT Events," *Proceedings of the IEEE International SoC Design Conference*, pp. 21-24, November 2010

49. R. Jakushokas, E. Salman, E. G. Friedman, R. M. Secareanu, O. L. Hartin, and C. Recker, "Compact Substrate Models for Efficient Noise Coupling and Signal Isolation Analysis," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2346-2349, May/June 2010

50. E. Salman and E. G. Friedman, "Methodology to Achieve Higher Tolerance to Delay Variations in Synchronous Circuits," *Proceedings of the ACM/IEEE Great Lakes Symp. on VLSI*, pp. 447-452, May 2010

51. E. Salman and E. G. Friedman, "Reducing Delay Uncertainty in Deeply Scaled Integrated Circuits Using Interdependent Timing Constraints," *Proceedings of the ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, pp. 77-82, March 2010

52. Kose, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power Ground Noise," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2277-2280, May 2009

53. E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Contact Merging Algorithm for Efficient Substrate Noise Analysis in Large Scale Circuits," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 9-14, May 2009

54. S. Kose, E. Salman, Z. Ignjatovic, and E. G. Friedman, "Pseudo-Random Clocking to Enhance Signal Integrity," *Proceedings of the IEEE International System-on-Chip Conference*, pp. 47-50, September 2008

55. E. Salman and E. G. Friedman, "Methodology for Placing Localized Guard Rings to Reduce Substrate Noise in Mixed Signal Circuits," *Proc. of the 4th Conf. on PhD Research in Microelectronics and Electronics*, pp. 85-88, June 2008

56. E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Input Port Reduction for Efficient Substrate Extraction in Large Scale ICs," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 376-379, May 2008

57. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Equivalent Rise Time for Resonance in Power/Ground Noise Estimation," *Proc. of the IEEE International Symposium on Circuits and Systems*, pp. 2422-2425, May 2008

58. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Dominant Substrate Noise Coupling Mechanism for Multiple Switching Gates," *Proc. of the IEEE Int. Symposium on Quality Electronic Design*, pp. 261-266, March 2008

59. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Substrate Noise Reduction Based On Noise Aware Cell Design," *Proc. of the IEEE International Symposium on Circuits and Systems*, pp. 3227-3230, May 2007, **invited paper**

60. E. Salman, E. G. Friedman, and R. M. Secareanu, "Substrate and Ground Noise Interactions in Mixed-Signal Circuits," *Proceedings of the IEEE International System-on-Chip Conference*, pp. 293-296, September 2006

61. E. Salman, A. Dasdan, F. Taraporevala, K. Kucukcakar, and E. G. Friedman, "Pessimism Reduction in Static Timing Analysis Using Interdependent Setup and Hold Times," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 159-164, March 2006, **nominated for the best paper award**

62. E. Salman, H. Akin, O. Gursoy, A. Ergintav, I. Tekin, A. Bozkurt, and Y. Gurbuz, "Design of a 3.2 mW PLL Based Clock and Data Recovery Circuit in 90-nm CMOS Technology," *Proceedings of the Mediterranean Microwave Symposium*, September 2005

- **Nonrefereed Publications and Reports**

63. W. Liu, C. Sitik, E. Salman, B. Taskin, S. Sundareswaran, and B. Huang, "Slew-Driven Clock Tree Synthesis (SLECTS) Methodology to Facilitate Low Voltage Clocking," *Semiconductor Research Corporation (SRC) Technology Conference (TECHCON)*, September 2016

64. T. Wan, Y. Karimi, E. Salman, and M. Stanacevic, "A New Circuit Design Framework for IoT Devices," *International Conference and Expo on Emerging Technologies for a Smarter World*, October 2015

65. W. Liu, E. Salman, C. Sitik, B. Taskin, S. Sundareswaran, and B. Huang, "Circuits and Algorithms to Facilitate Low Swing Clocking in Nanoscale Technologies," *Semiconductor Research Corporation (SRC) Technology Conference (TECHCON)*, September 2015

66. E. Salman and M. Stanacevic, "3-D Integrated Implantable Device for Deep Brain Sensing and Stimulation," *International Conference and Expo on Emerging Technologies for a Smarter World*, November 2011

67. G. Bischof, B. Scholnick, and E. Salman, "Fully Integrated PLL Based Clock Generator for Implantable Biomedical Applications," *IEEE Annual Conference on Long Island Systems, Applications and Technology*, May 2011

68. E. Salman, A. Doboli, and M. Stanacevic, "Noise and Interference Management in 3-D Integrated Wireless Systems," *International Conference and Expo on Emerging Technologies for a Smarter World*, September 2010

Invited Talks Tutorials

- Back to the "War of Currents": Can AC Computing be an Alternative for Wirelessly Powered Devices?, Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY, May 2017
- Low Voltage Clocking as a Practical Low Power Design Strategy for Industrial Circuits, Samsung Austin Research Center (SARC), Austin, TX, November 2016
- VLSI Design Beyond 50^{th} Anniversary of Moore's Law, Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, NY, September 2016
- Design and Automation of a Novel Low Swing Clocking Methodology with Reduced Delay Uncertainty, Semiconductor Research Corporation Design Review, Dallas, TX, November 2015
- Circuits and Algorithms to Facilitate Low Swing Clocking in Nanoscale Technologies, September 2015
  - Advanced Micro Devices (AMD) Inc., Austin, TX
  - Freescale Semiconductor Inc. (Now NXP Semiconductors), Austin, TX
- Low Voltage Power Delivery and Clocking in Nanoscale Technologies: Basics to Recent Advances, Lisbon, Portugal, May 2015 (with Baris Taskin)
  - Three-hour long tutorial at IEEE International Symposium on Circuits and Systems
- Challenges and Opportunities in 3D Integrated Circuits, IEEE Long Island, Farmingdale, NY, April 2015
- New Milestony in Wireless Energy Harvesting, Simon's Foundation, New York, NY, December 2014
  - TED-type talk to a diverse audience of over 100 people and distinct judges including Nobel laureate Peter Agre for 2014 Discovery Prize Competition
- Design and Automation of a Novel Low Swing Clocking Methodology with Reduced Delay Uncertainty, Semiconductor Research Corporation Design Review, UC Berkeley, CA, October 2014.
- Ensuring Power and Signal Integrity in Heterogeneous 3D ICs, Workshop on 2.5D/3D Technology and Design Enablement for Heterogeneous Systems, Nanyang Technological University, Singapore, July 2013
- Robust Power Delivery in TSV Based 3D Processor-Memory Stacks, CASS Forum on Emerging and Selected Topics (CAS-FEST), Heterogeneous Nano-Circuits and Systems, Seoul, South Korea, May 2012
- Noise Management in Highly Heterogeneous SoC Based Integrated Circuits, IEEE International SoC Design Conference, Seoul, South Korea, November 2010
- Noise-Centric Physical Design Methodologies for VLSI Based Nanoscale Systems, March-April 2010.
  - University of Maryland
  - University of Miami
  - University of Pittsburgh
  - Stony Brook University (SUNY)

  - University of Alaska
- Switching Noise and Timing Considerations in Nanoscale Integrated Circuits, Microelectronics Group, Sabanci University, Istanbul, Turkey, June 2008
- Substrate Noise Reduction Based on Noise Aware Cell Design, IEEE International Symposium on Circuits and Systems, New Orleans, LA, May 2007
- Impact of Substrate on Ground Noise, Microwave and Mixed-Signal Technologies Laboratory, Freescale Semiconductor Inc., Tempe, AZ, February 2006.

Professional Activities

- **Memberships**
  - Senior Member, IEEE, 2017 to present
  - Member, IEEE, 2003 to 2017
  - Member, IEEE Circuits and Systems Society, 2013 to present
  - Technical committee member, VLSI Systems and Applications, IEEE Circuits and Systems Society, 2015 to present
- **Editorial Activities**
  - Regional editor, Journal of Circuits, Systems and Computer, July 2013 to present
    - One of the five managing editors of the journal
  - Associate editor, Journal of Low Power Electronics and Applications, 2010 to present
  - Associate editor, IEEE Trans. on Very Large Scale Integration (VLSI) Systems, 2011 to 2015
- **Conference and Organizational Activities**
  - Special sessions chair, ACM/IEEE Great Lakes Symposium on VLSI, 2017
  - Finance chair, ACM/IEEE System Level Interconnect Prediction, 2016
  - Registration chair, ACM/IEEE Great Lakes Symposium on VLSI, 2016
  - Publicity chair, ACM Design Automation Conference PhD Forum, 2012
- **Technical Program Committees**
  - ACM/IEEE System Level Interconnect Prediction
  - IEEE Conference on Electron Devices and Solid-State Circuits
  - IEEE International Symposium on Quality Electronic Design
  - ACM/IEEE Great Lakes Symposium on VLSI, 2010 to present
  - ACM/IEEE Asia Symposium on Quality Electronic Design
  - IEEE International Symposium on Electronic System Design
  - IEEE International Conference on Microelectronics
  - First Int. Workshop on Secure and Resilient Architectures and Systems
  - First Int. Workshop on Thermal Modeling and Management: From Chips to Datacenters
- **Special Sessions**
  - Energy-Efficient and Secure IoT, IEEE Int. Symposium on Circuits and Systems, 2017
  - Circuit and System Design for Emerging IoT Applications, IEEE Int. Symposium on Circuits and Systems, 2016
- **Session Chair/Co-Chair**
  - Energy Efficient and Secure IoT, IEEE International Symposium on Circuits and Systems, 2017
  - Advanced Digital Techniques, IEEE International Symposium on Circuits and Systems, 2017

  - Networks-on-Chip, IEEE International Symposium on Circuits and Systems, 2017
  - Emerging IoT, IEEE International Symposium on Circuits and Systems, 2016
  - Integration Issues, IEEE International Symposium on Circuits and Systems, 2016
  - VLSI-I, IEEE International Symposium on Circuits and Systems, 2016
  - VLSI Design, ACM/IEEE Great Lakes Symposium on VLSI, 2015
  - Sensors, IEEE International Symposium on Circuits and Systems, 2012
  - Nanorobotics and Nano-Giga Circuits, IEEE Int. Symposium on Circuits and Systems, 2011
  - VLSI Circuits, ACM/IEEE Great Lakes Symposium on VLSI, 2010
- **Reviewer**
  - IEEE Transactions on Very Large Scale Integration Systems
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
  - IEEE Transactions on Nanotechnology
  - IEEE Transactions on Circuits and Systems-I
  - IEEE Transactions on Circuits and Systems-II
  - IEEE Journal on Emerging Selected Topics in Circuits and Systems
  - IEEE Embedded Systems Letters
  - Integration, the VLSI Journal
  - Elsevier Microelectronics Journal
  - Springer Analog Integrated Circuits and Signal Processing

Teaching Activity

- ESE 585 Nanoscale Integrated Circuit Design (Spring semesters)
  - New course to the graduate curriculum
  - Average number of students: 16
  - Emphasis on interconnect-centric IC design process (data, power, and clock networks)
- ESE 555 Advanced VLSI Systems Design (Fall semesters)
  - Average number of students: 46
  - Traditional VLSI course with emphasis on combinational and sequential circuits, data paths
- ESE 324 Electronics Laboratory C (Spring semesters)
  - Redesigned the entire course and experiments
  - Average number of students: 58
  - Experimental lab course with emphasis on PLLs, data converters, DC-DC voltage converters
- ITS 102 Introduction to Modern Chip Design (Spring 2015)
  - New seminar course open to university-wide freshmen population, 18 students
- ESE 670 Topics in Electrical Sciences (Fall 2010)

Service and Outreach

- **Departmental Service**
  - Industry Liaison, 2016-present
    - Coordinating the Department's relationships with the corporate world
  - Graduate Committee Member, 2016-present
  - ECE Chair Search Committee Member, 2016
  - Undergraduate Committee Member, 2011 to 2016
  - Graduate Admissions Committee Member, 2011 to 2015
  - Committee Member for PhD Qualifying Exam in VLSI and Circuits, 2011-present
  - ABET Assessment Committee Chair for ESE 324, 2011 to present
  - Member of Various PhD Dissertation Defense Committees, 2010-present
  - Panelist at Graduate School Discussion for ECE Honors Students, 2013
  - Panelist at ECE Honors Seminar on Theory versus Experiment, 2015
- **College Service**
  - Information and Technology Studies (ITS) 102 Instructor, 2015
  - Information and Technology Studies (ITS) Round Table: Chat with Professors, 2012
  - Panelist at the New Teaching Assistant Orientation, 2011
- **Outreach Activities**
  - Co-organizer, Engineering Enterprise, 2015
    - Year-long program to educate underrepresented high school students from high-needs school districts
    - Longer exposure of the students to the field of electrical and computer engineering
    - Received Outreach Initiative Award from IEEE CASS to partially support this activity
  - Co-organizer and instructor, Summer Engineering Camp, 2012, 2013, and 2014
    - Two-week residential camp to introduce selected high school students with diverse engineering projects
    - Received Outreach Initiative Award from IEEE CASS to partially support this activity
  - Judge at Research Association Invitational Science Fair, 2012

Graduate Students

- **PhD Alumni**
  - Dr. Weicheng Liu, January 2018
    - First position: NXP Semiconductors, Austin, TX
    - Dissertation: Low Voltage Clocking Methodologies for Nanoscale ICs
  - Dr. Zhihua Gan, August 2017
    - First position: Nordco, Beacon Falls, CT
    - Dissertation: Design Methodologies to Manage Switching Noise with Applications to Biomedical Acoustic Systems
  - Dr. Hailang Wang, January 2016
    - First position: Apple Inc., Cupertino, CA
    - Dissertation: Enhancing Power and Signal Integrity in Three-Dimensional Integrated Circuits
- **Current PhD Students**
  - Chen Yan, expected February 2019
  - Tutu Wan, expected May 2019

- Manav Jain, expected May 2021
- Mallika Rathore, expected May 2021
- Ivan Miketic, expected May 2022
- Libo Wu (co-advised with Prof. Ya Wang, Mechanical Eng.), expected May 2021

- **MSc Alumni with Thesis**
  - Yongwan Park, May 2016
    - First position: Ph.D. student at University of Maryland College Park
    - Thesis: Fully Integrated Hybrid Voltage Regulator for Low Voltage Applications
  - Sushil Panda, May 2016
    - First position: Dolphin Technology, Santa Clara, CA
    - Thesis: Investigating the Tolerance of Wirelessly Powered Charge-Recycling Logic to Power-Clock Phase Difference Deviations
  - Tasnuva Noor, May 2016
    - First position: Brookhaven National Laboratory, Brookhaven, NY
    - Thesis: Design of a Novel Glitch-Free Integrated Clock Gating Cell for High Reliability
  - Mallika Rathore, May 2014
    - First position: Marvell Semiconductor, Boise, ID
    - Thesis: Design and Analysis of Custom Clock Buffers and a D Flip-Flop for Low Swing Clock Distribution Networks
  - Peirong Ji, December 2013
    - First position: SK Hynix, San Jose, CA
    - Thesis: Quantifying the Effect of Local Power Distribution Network and Vias on Power Integrity
  - Sateja Mungi, May 2013
    - First position: Intel Corporation, Hudson, MA
    - Thesis: Effective Distance Calculations for On-Chip Decoupling Capacitors in 3D ICs
  - Ziqi Zhang, May 2013
    - First position: Marvell Semiconductor, San Jose, CA
    - Thesis: Comparative Analysis of Near-Threshold and Charge Recovery Circuits for Energy Efficiency and Performance
  - Ajay Chandrasekhar, May 2013
    - First position: Imagination Technologies, San Jose, CA
    - Thesis: Critical Length Estimation for TSV-Based 3D Sub/Near-Threshold Circuits
  - Suhas M. Satheesh, May 2012
    - First position: NVIDIA, Santa Clara, CA
    - Thesis: Power Distribution in TSV Based 3D Processor-Memory Stacks
  - Mohammad H. Asgari, December 2011
    - First position: Ph.D. student at Columbia University, New York, NY
    - Thesis: TSV Related Noise Coupling in 3D Integrated Circuits

- **Undergraduate Research and Advising**
  - Seongmin Han, 2016-2017
    - Senior design project
  - Scott Kontak, 2016-2017

  - NSF REU scholarship
  - Co-author of several IEEE/ACM papers
  - First position: Ph.D. student at Columbia University, NY
- Xiaoxi Zhang, 2016-2017
  - ECE Honors research
  - First position: Signal Integrity Engineer at Intel, Hillsboro, OR
- Joram Mercado, 2015-2017
  - Senior design project
  - Independent research
  - First position: M.Sc. student at Stony Brook University
- Jea Won Kwon, 2015-2016
  - Senior design project
- Yongwan Park, 2014-2015
  - NSF REU scholarship
  - First author of an IEEE ISCAS 2016 paper
  - First position: M.Sc. student at Stony Brook University, Ph.D. student at University of Maryland
- Shiwei Fang, 2013-2014
  - ECE honors research
  - First author of an IEEE ISCAS 2015 paper
  - Recipient of Provost Award for Academic Excellence
  - Recipient of Undergraduate Recognition Award
  - First position: Ph.D. student at University of North Carolina at Chapel Hill
- Sung Jun Yoon, 2012-2013
  - URECA (Undergraduate Research and Creative Activities) fellowship
  - Co-author of an ACM journal paper
  - First position: Ph.D. student at Texas A&M University
- Jongmun Hwang, 2012-2013
  - Senior design project
- Artem Ayzen, 2011-2012
  - Senior design project
- Garrett Bischoff, 2010-2011
  - Senior design project
  - First author of a LISAT 2011 paper
- Ben Scholnick, 2010-2011
  - Senior design project
  - Co-author of a LISAT 2011 paper