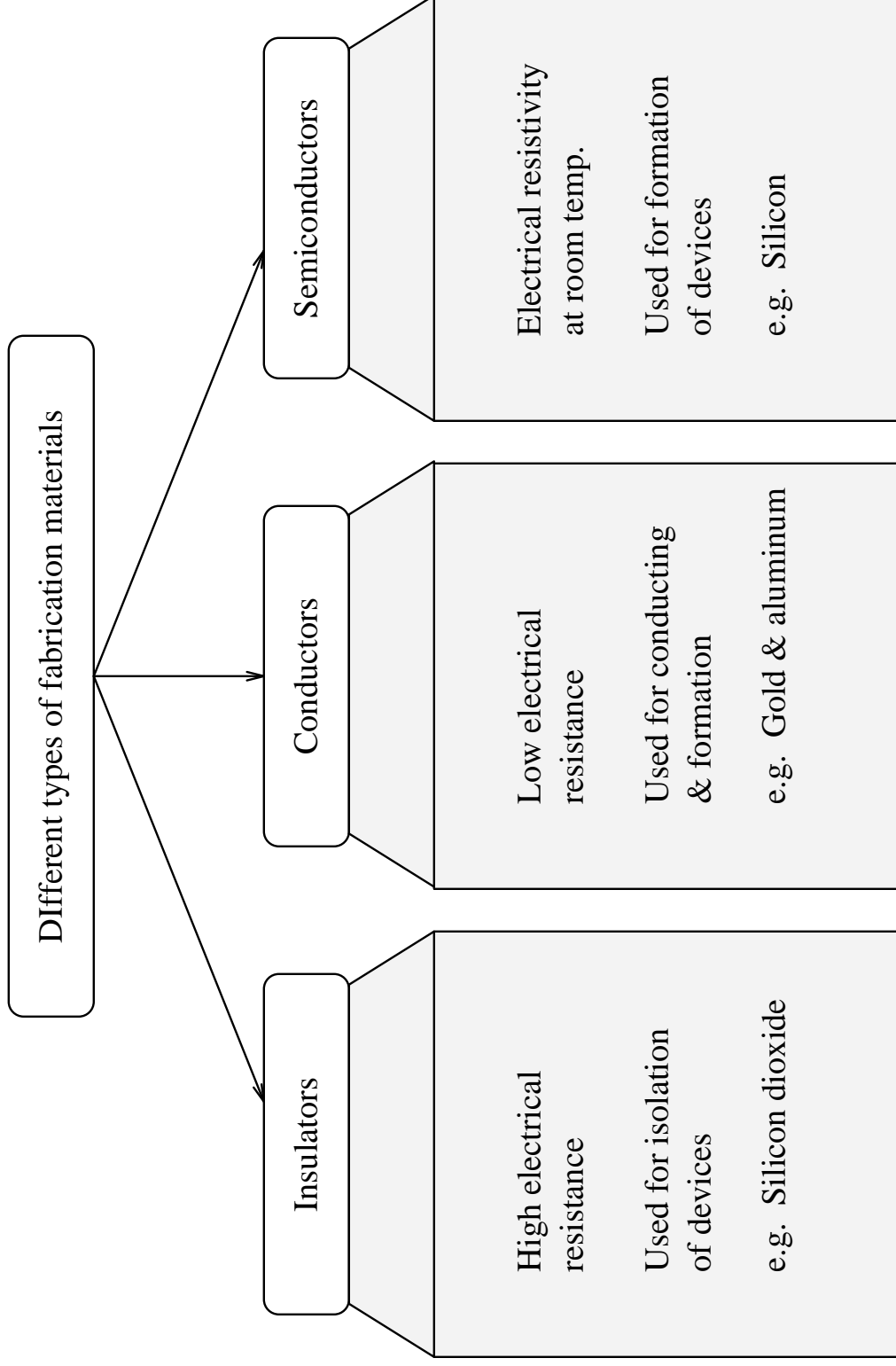


Design and Fabrication of VLSI Devices

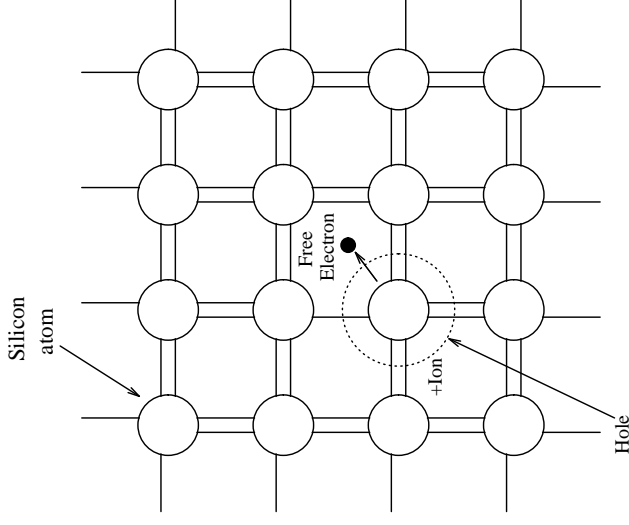
Objectives:

- To study the materials used in fabrication of VLSI devices.
- To study the structure of devices and process involved in fabricating different types of VLSI circuits.

Fabrication Materials

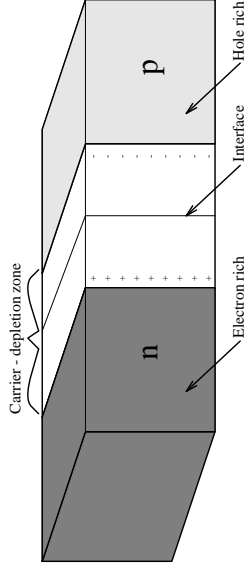


Electrons and Holes

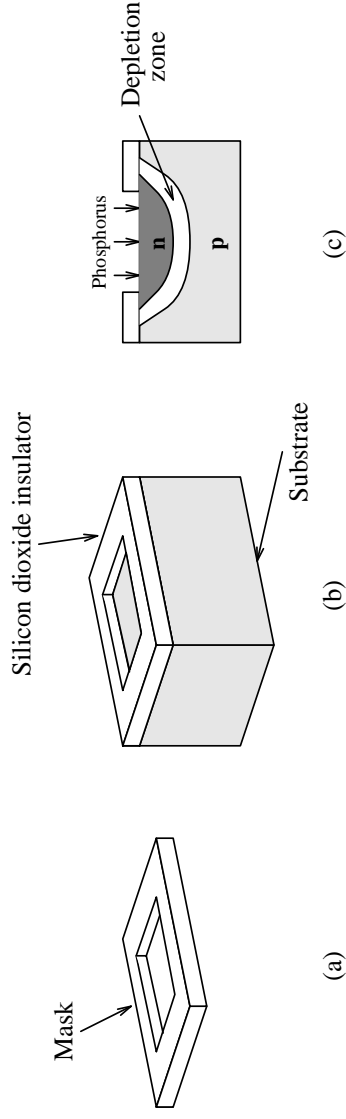


- Holes travel as do electrons.
- Material can be enriched in holes or electrons by introducing impurities.
- Holes in crystals can be enriched by embedding some boron atoms.
- Electrons in crystals can be enriched by embedding phosphorus atoms.

The Three Regions in a n-p Junction

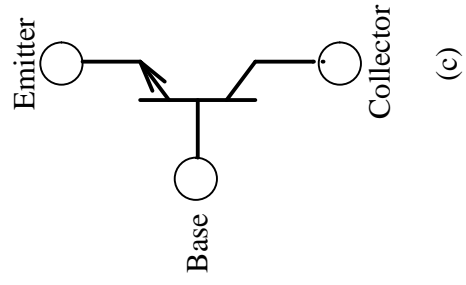
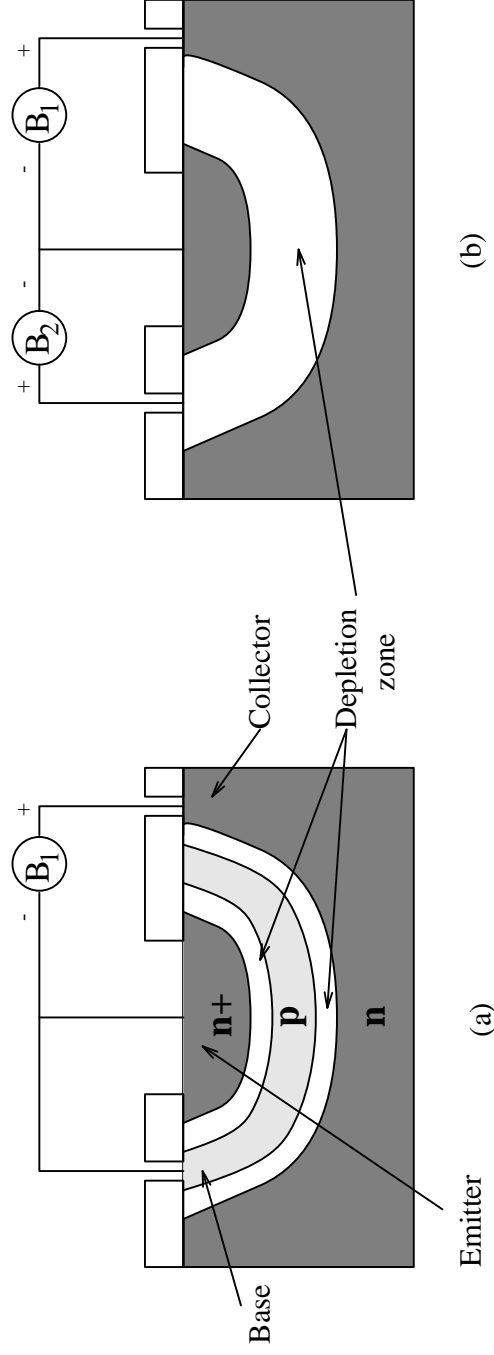


Formation of a Diffused Junction



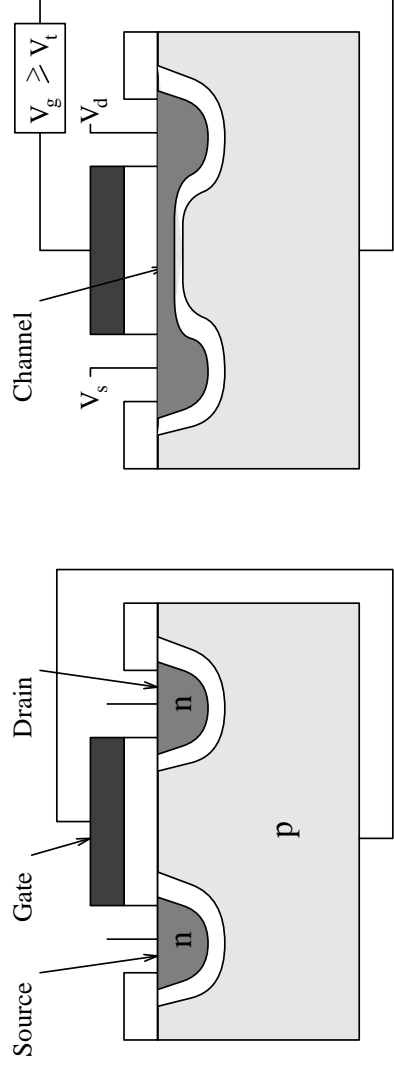
A *mask* is a specification of geometric shapes that need to be created on a certain layer. Masks are used to create specific patterns of each material in a sequential manner and create a complex pattern of several layers.

TTL Transistor

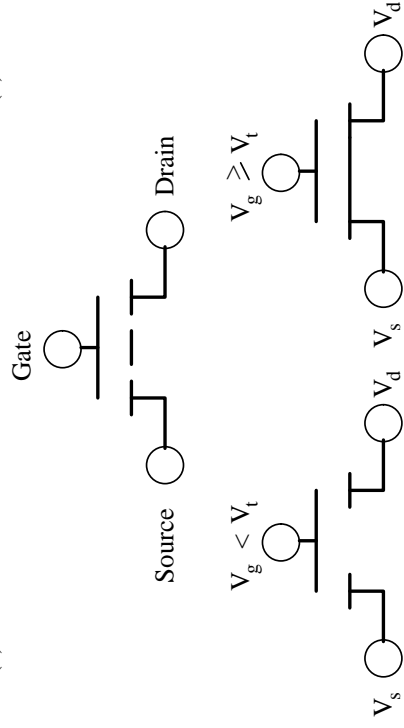


A nMOS Transistor

Enhancement Mode



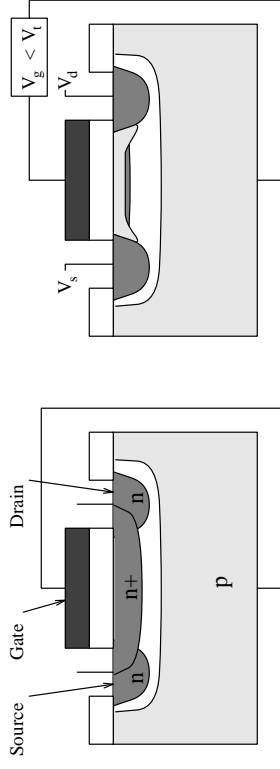
(a) (b)



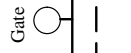
(c)

A nMOS Transistor

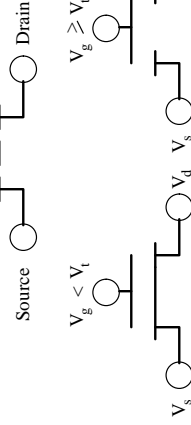
Depletion Mode



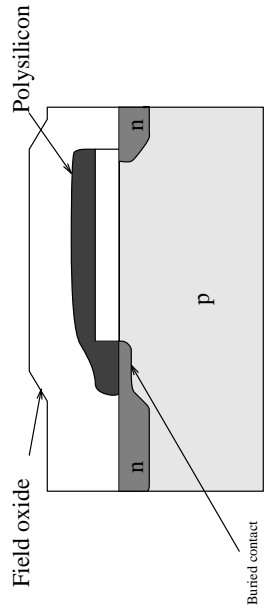
(a)



(b)



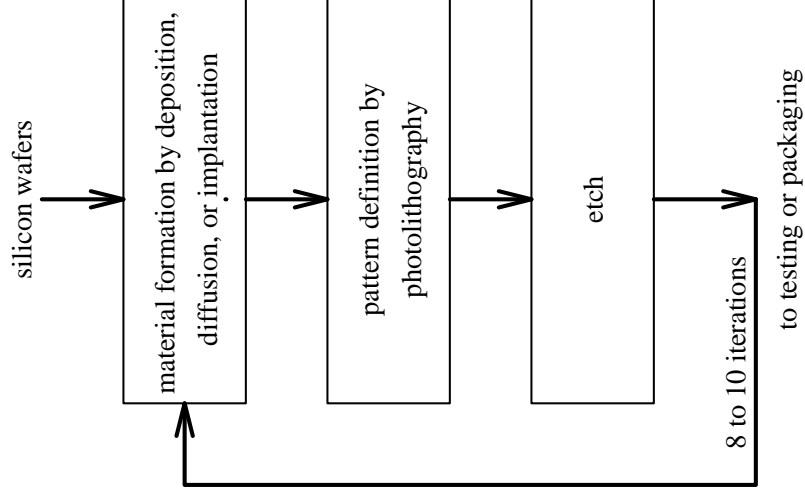
(c)



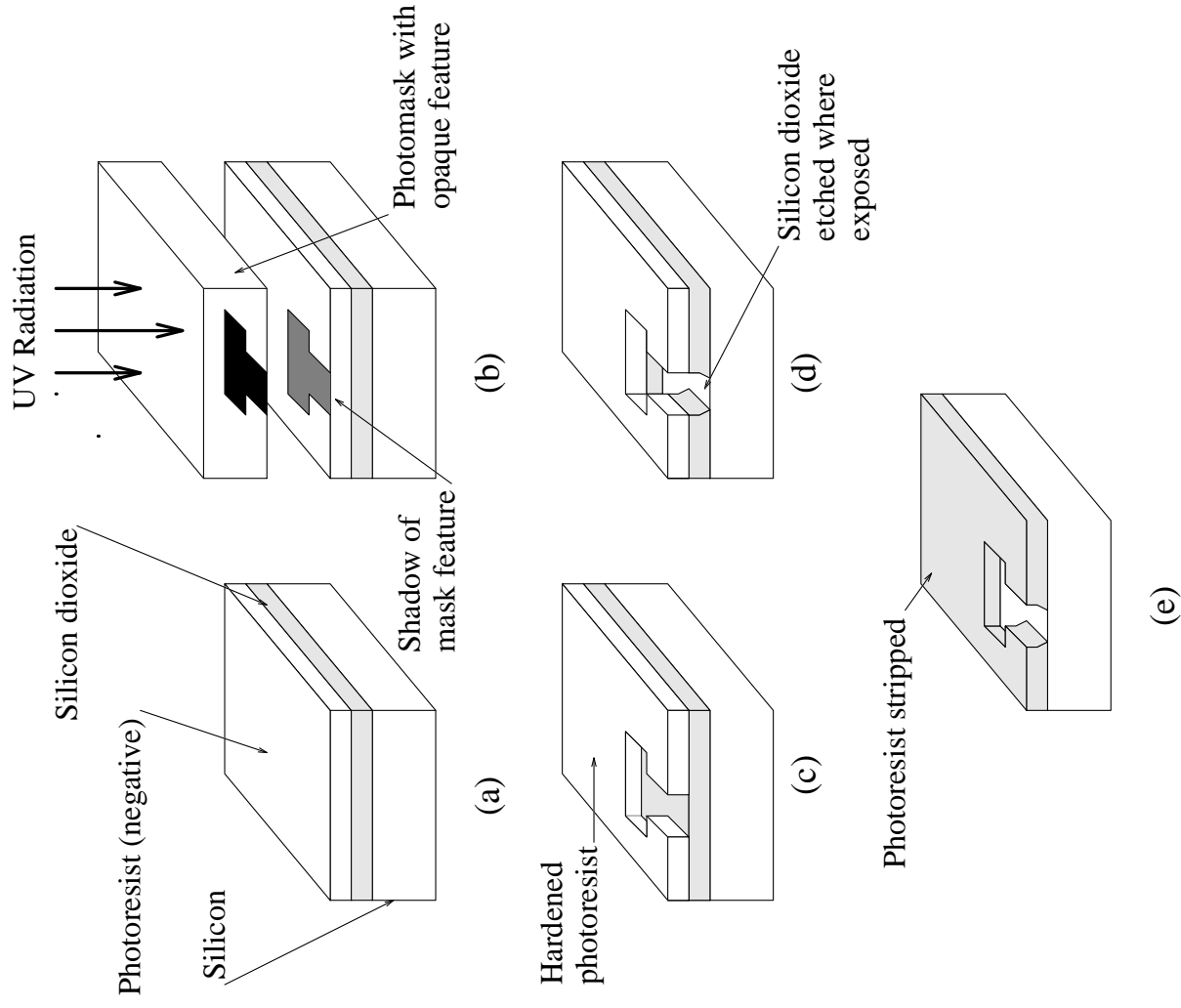
(d)

Fabrication of VLSI Circuits

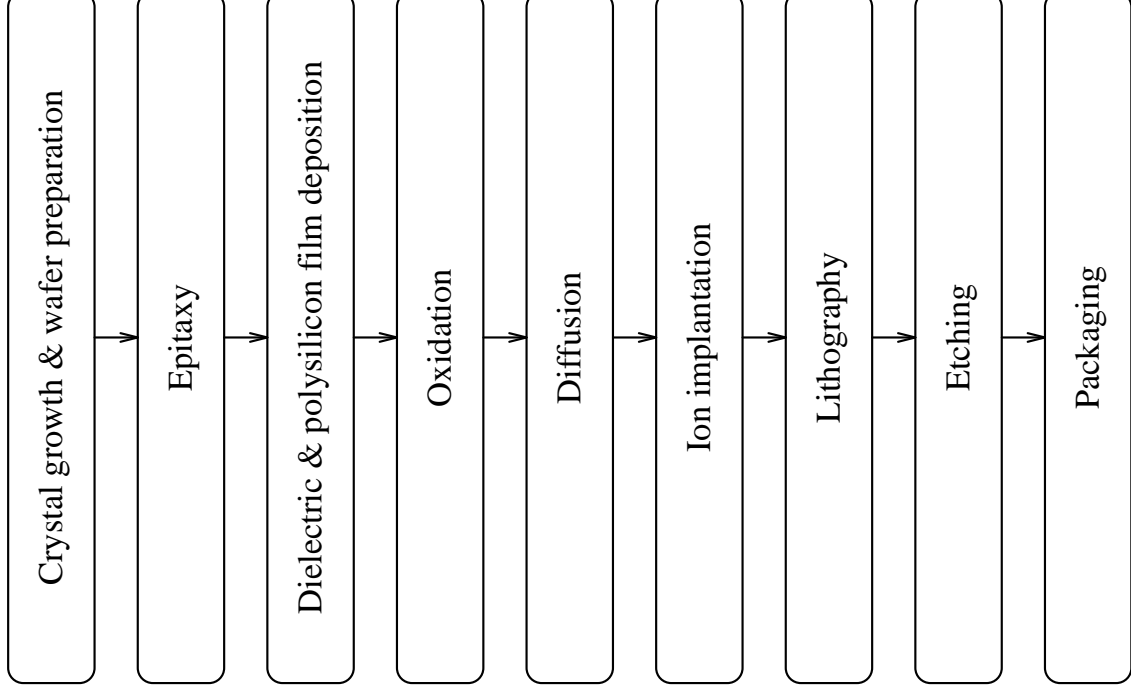
1. Create
2. Define
3. Etch



Photolithographic Process



Details of Fabrication Processes



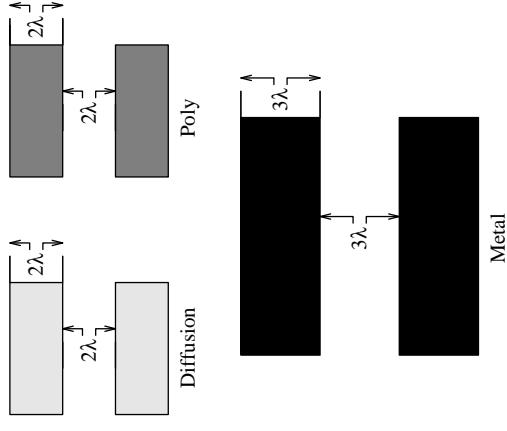
Basic Design Rules

1. Size Rules
2. Separation Rules
3. Overlap Rules

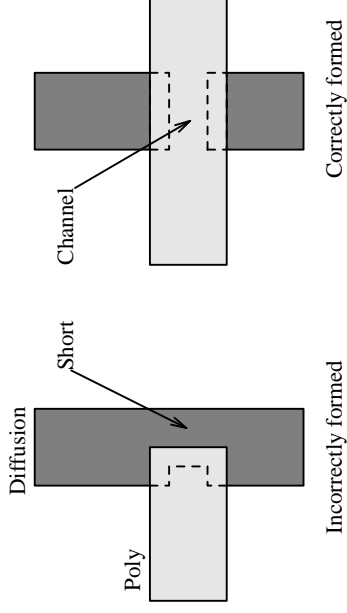
Basic nMOS Design Rules

| | |
|-----------------------------|------------|
| Diffusion Region Width | 2λ |
| Polysilicon Region Width | 2λ |
| Diffusion-Diffusion Spacing | 3λ |
| Poly-Poly Spacing | 2λ |
| Polysilicon Gate Extension | 2λ |
| Contact Extension | λ |
| Metal Width | 3λ |

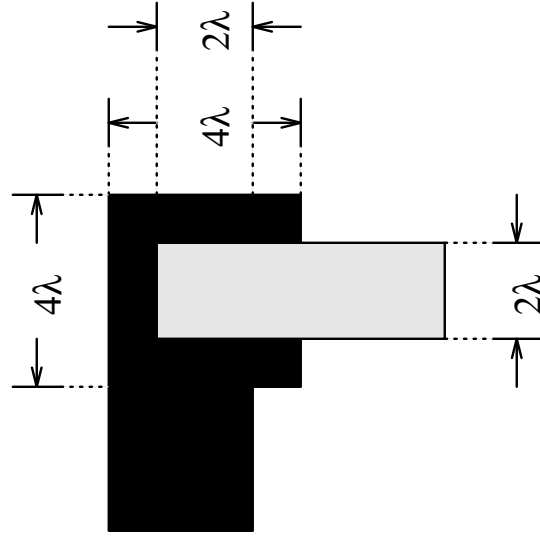
Size and Separation Rules



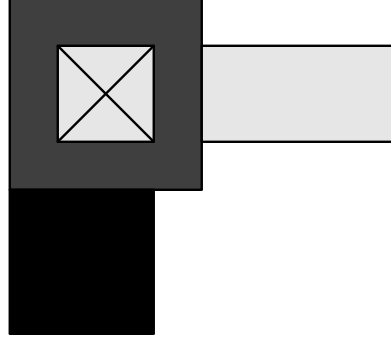
Incorrectly and Correctly Formed Channels



Overlap Rules for Contact Cuts



(a)



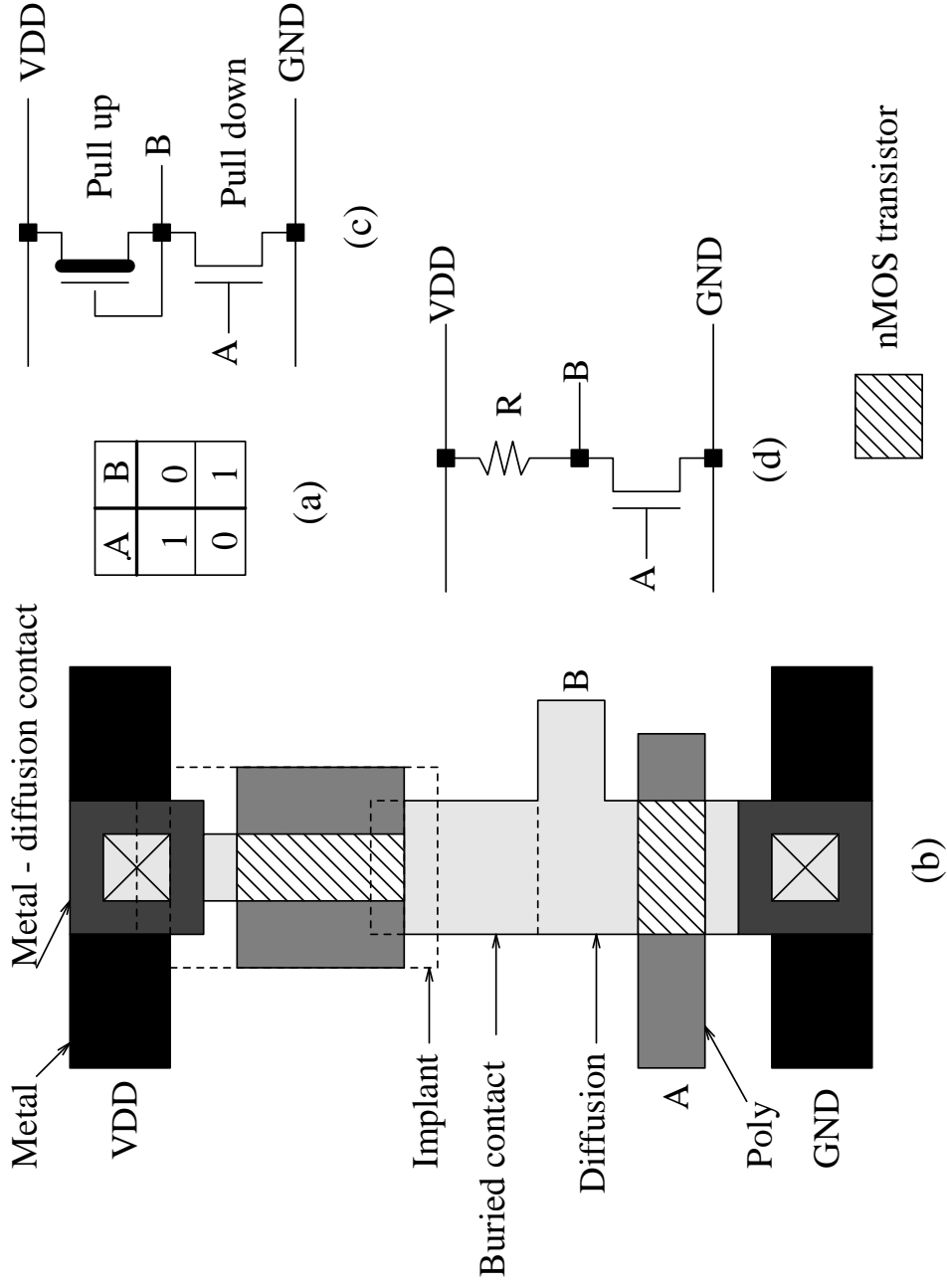
(b)

Layout of Basic Devices

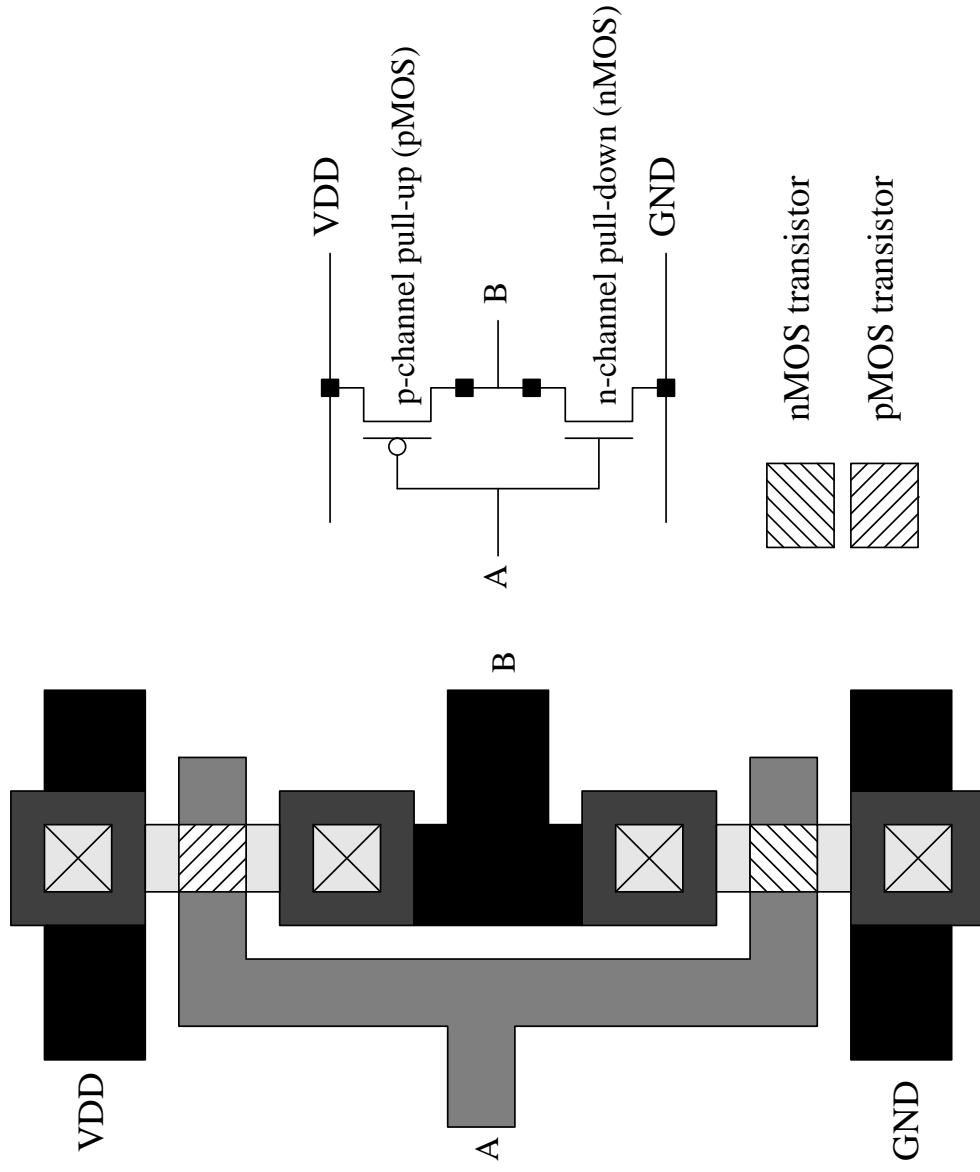
- nMOS Inverter
- CMOS Inverter
- nMOS NAND Gate
- nMOS NOR Gate
- CMOS NAND Gate
- CMOS NOR Gate

Complicated devices are constructed by using basic devices.

An nMOS Inverter



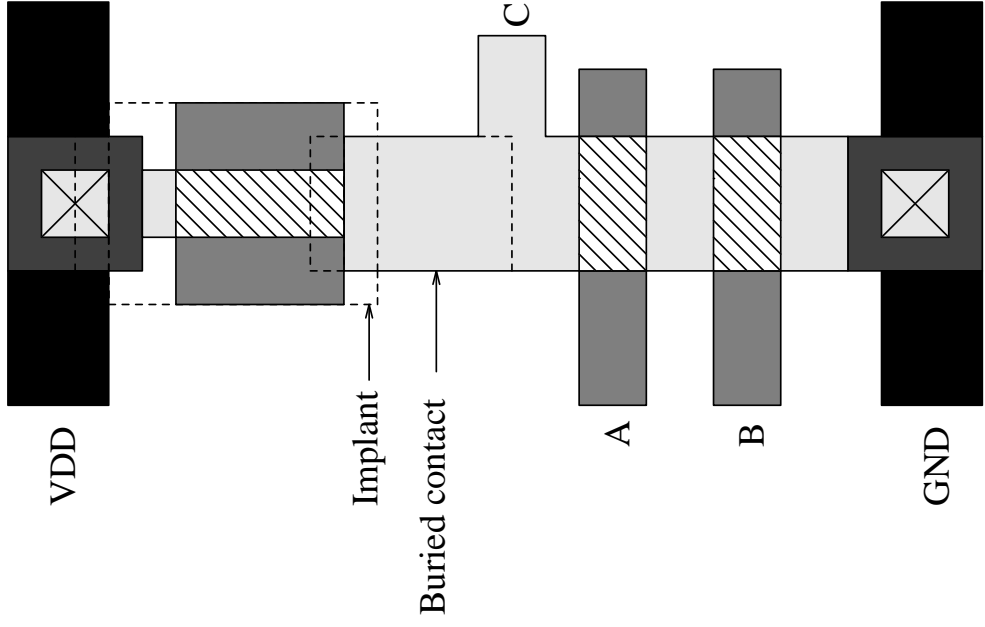
A CMOS Inverter



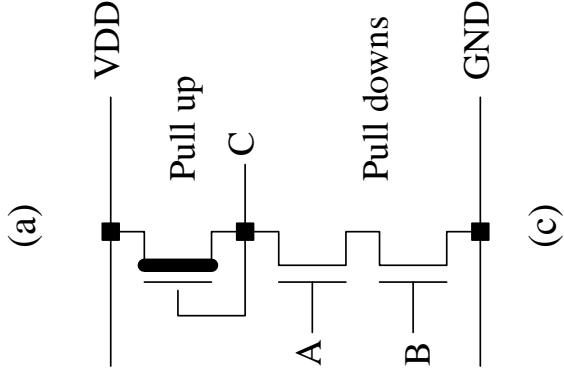
Comparison of CMOS and MOS Characteristics

| CMOS | MOS |
|---|--|
| Zero static power dissipation | Power is dissipated in the circuit with output of gate at '0' |
| Power dissipated during logic transition | Power dissipated during logic transition |
| Requires 2N devices for N inputs for complementary static gates | Requires (N+1) devices for N inputs |
| CMOS encourages regular layout styles | Depletion, load and different driver transistors create irregularity in layout |

A nMOS NAND Gate

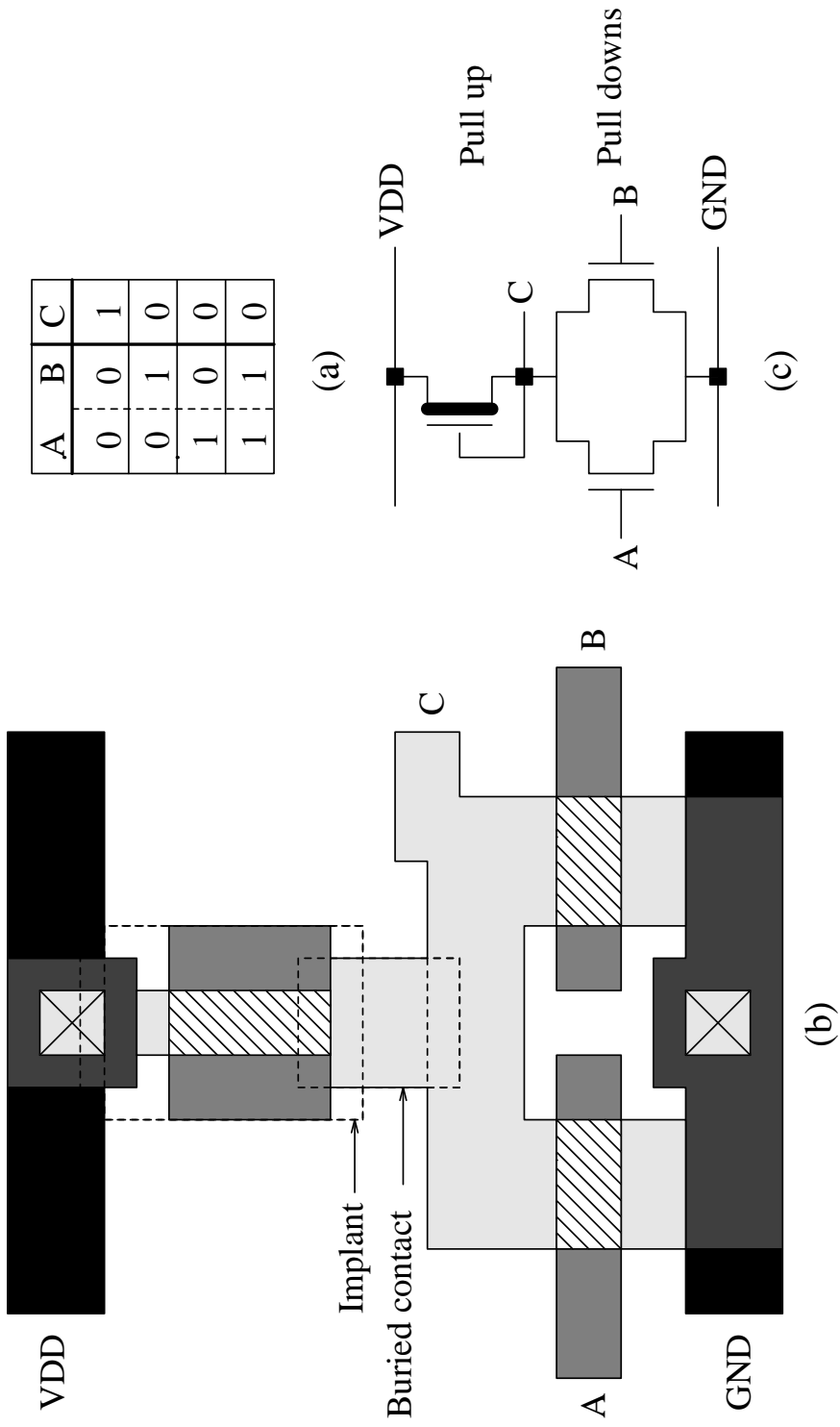


| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

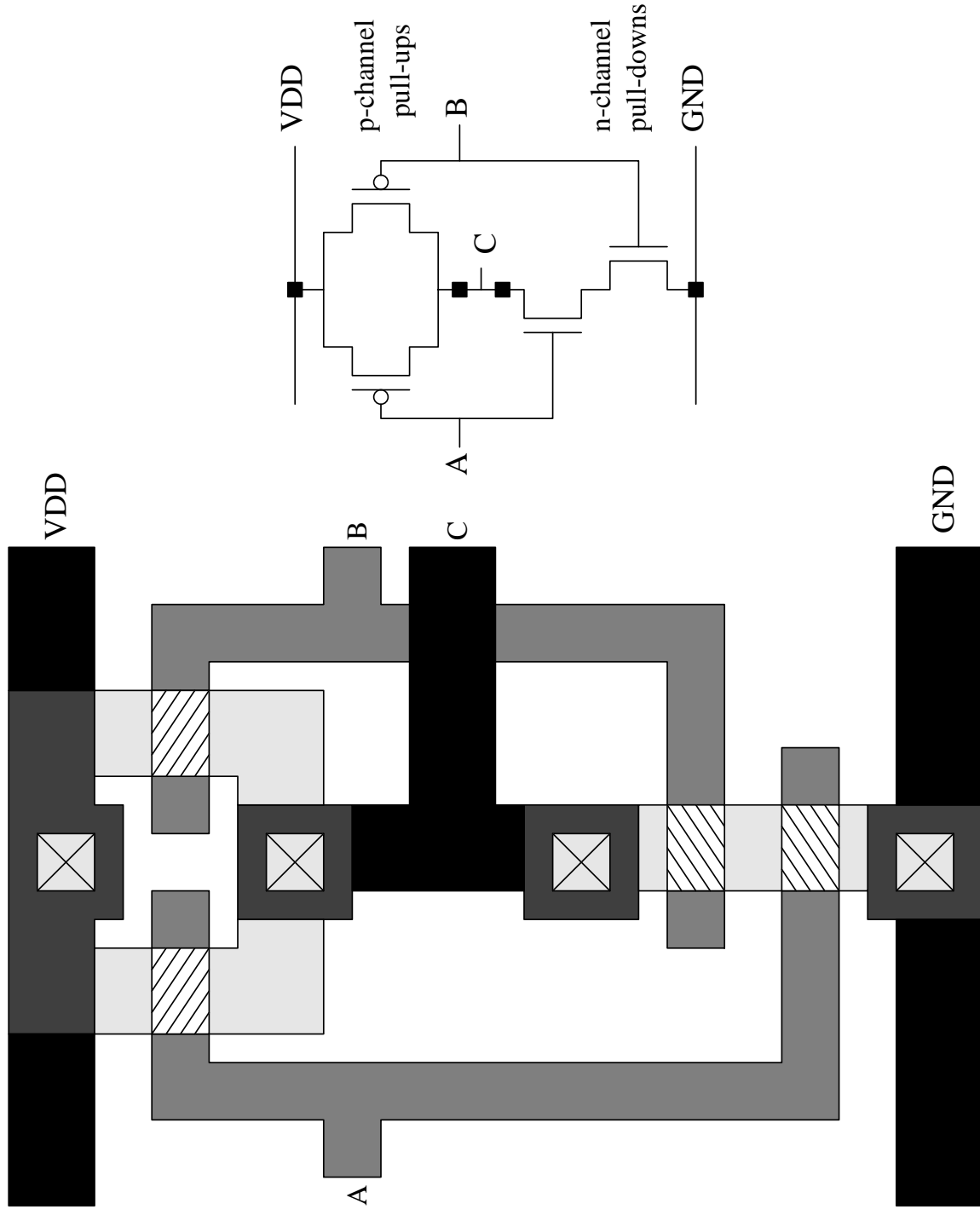


(b)

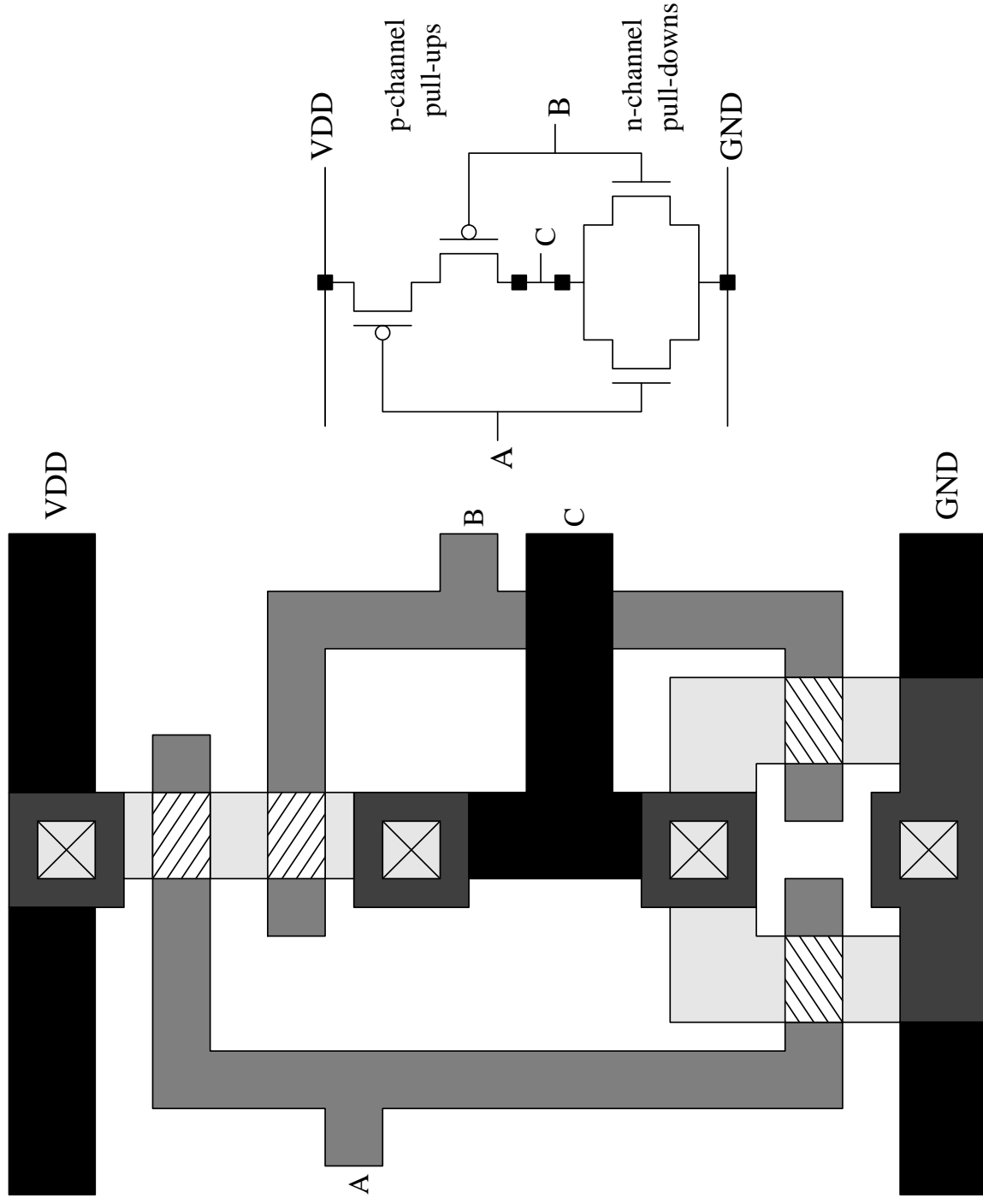
A nMOS NOR Gate



A CMOS NAND Gate



A CMOS NOR Gate



Additional Fabrication Factors

- Scaling
- Parasitic Effects
- Yield Statistics and Fabrication Costs
- Delay Computation
- Noise and Crosstalk
- Power Dissipation

Scaling and Parasitic Effects

The process of shrinking the layout, in which every dimension is multiplied by a factor is called *scaling*.

| Parameter | Full scaling | CV scaling |
|--|--------------|------------|
| Dimensions: width, length, oxide thickness | $1/S$ | $1/S$ |
| Voltages: Power, threshold | $1/S$ | 1 |
| Gate capacitance | $1/S$ | $1/S$ |
| Current | $1/S$ | S |
| Propagation delay | $1/S$ | $1/S^2$ |

Parasitic effects includes the stray capacitance, the capacitance between the signal paths and ground, and the inherent capacitance of the MOS transistor.

Yield Statistics and Fabrication Costs

Yield of a chip depends on size of the chip and maturity of the process

$$C_{ud} = \frac{C_w}{N_d * Y}$$

N_d =number of dies (chips) fit into a wafer

C_{ud} =cost of an untested die, C_w =cost of wafer fabrication,

Y =probability of a die being functional after processing.

$$N_d = \pi \frac{(D - \alpha)^2}{4X^2}$$

D =diameter of the wafer,

α =useless scrap edge distance of a wafer, X =chip dimension.

Yield Statistics and Fabrication Costs

$$Y = (1 - A\delta/c)^c$$

Y =yield, A =area of a single chip,

δ =defect density, c =parameter that indicates defect clustering.

$$N_g = \frac{(X^2 - P * A_{io})}{A_g}$$

N_g =number of gates in a single IC,

P =number of pads on the chip surface, A_g =area of a logic gate,

A_{io} =area of an I/O cell.

$$P = 4(X/S - 1)$$

S =the minimum pad to pad pitch,

P =number of pads required to connect the chip to next level of interconnect.

Delay Computation

$$R = \frac{\rho l_c}{h_c w_c}$$

ρ =resistivity, w_c , h_c , and l_c are the width, thickness, and length of the conductor. R =resistance of a uniform slab of conducting material.

$$C = \left[1.15 \left(\frac{w_c}{t_o} \right) + 2.80 \left(\frac{h_c}{t_o} \right)^{0.222} + \left[0.06 \left(\frac{w_c}{t_o} \right) + 1.66 \left(\frac{h_c}{t_o} \right) - 0.14 \left(\frac{h_c}{t_o} \right)^{0.222} \right] \left(\frac{t_o}{w_{ic}} \right)^{1.34} \right] \epsilon_s \epsilon_o l_c$$

C =capacitance of the conductor, w_{ic} =spacing of chip interconnections, t_o =thickness of the oxide, ϵ_s =permittivity of free space, ϵ_o =dielectric constant of the insulator.

Noise Crosstalk

Noise principally stems from resistive and capacitive coupling.

Noise margin is defined in terms of two parameters:

Low Noise Margin(LNM) and High Noise Margin(HNM).

$$LNM = \max(V_{IL}) - \max(V_{OL})$$

$$HNM = \min(V_{OH}) - \min(V_{IH})$$

Where V_{IL} and V_{IH} are low and high input voltages and V_{OL} and V_{OH} are low and high output voltages respectively.

One of the forms of noise is crosstalk, which is a result of mutual capacitance and inductance between neighboring lines.

Power Dissipation

- Temperature must be as uniform as possible over the entire chip surface.
- Heat generated must be efficiently removed from the chip surface.
- A CMOS gate uses $0.003 \text{ mW/MHz/gate}$ in ‘off’ state and 0.8 mW/MHz/gate during its operation.
- A ECL system uses 25 mW/gate irrespective of state and operating frequency.

Summary

1. The three types of materials are insulators, conductors, and semiconductors.
2. A VLSI chip consists of several layers of different materials on a silicon wafer.
3. Each layer is defined by a mask.
4. VLSI fabrication process patterns each layer using a mask.
5. Complex VLSI circuits can be developed using basic VLSI devices.
6. Design rules must be followed to allow proper fabrication.
7. Several factors such as scaling, parasitic effects, yield statistics and fabrication Costs, delay computation, noise and crosstalk, and power dissipation play a keyrole in fabrication of VLSI chips.