Spin orbit torque MRAM: Another myth or a soon-to-be reality?

Jean-Pierre Nozières, Gilles Gaudin, Marc Drouard, and Olivier Boulle
SPINTEC, CEA-INAC/CNRS/Univ.Grenoble-Alpes, 38054 Grenoble and
Antaios, Avenue Jean Kuntzmann, 38330 Montbonnot-Saint-Martin, France

For more than a decade, MRAM has been trumpeting the promise of a better (memory) world, with a technology that could replace DRAM, SRAM and (embedded) Flash. After a lot of twists and PR exercises from the players at stake, it appears that its latest incarnation, perpendicular spin transfer torque (STT) MRAM, is finally gearing towards product implementation. Given the attributes (or lack thereof) of the current technology, the targeted market is e-Flash replacement in data-intensive, energy-savvy applications such as IoT, automotive and mobile applications. Not quite the universal memory that was once envisioned, but definitely a step forward. Some major foundries have elected STT to be the embedded memory of choice for their sub-28 nm nodes. Whether STT is widely adopted by customers and breaks out of the "niche technology" doghouse remains to be seen, but the hopes are higher than ever.

Regardless of the forecast success, there is one thing that STT will never achieve: the performance required for processor-embedded cache memory. This is a market served today by SRAM, operating at close to GHz speed with infinite endurance (*e.g.* read/write cycles). For system designers, increasing the amount of on-chip SRAM is key to handle the ever-increasing amounts of data that have to be saved on-the-fly. However, after decades of the same approach, we are reaching physical and economic limits due to the combination of unsustainably high SRAM leakage currents at small technology nodes and high cost, with memory already accounting for more than 50% of the chip area. The development of an electrically addressable, zero-leakage memory technology combining processor clock speed, infinite endurance and easy integration with logic is perceived as a necessity.

Amongst the many emerging nonvolatile memory technologies, STT has been claiming it can do it all, from e-Flash to e-SRAM, by tweaking the materials and/or the bit cell layout. There is however a three-way tug of war that prevents achieving simultaneously speed, endurance and data retention in STT. Improving one degrades the others and *vice versa*. Claiming sub-5 ns reliable switching with better than a mere flash-like endurance is smoking grass.

We have recently proposed a novel memory concept, named spin-orbit torque (SOT) MRAM, that combines the advantages of STT with a truly infinite intrinsic endurance and a writing speed in the sub-ns regime. Bit-cell level proof of concept was demonstrated through static write and read and fast bipolar switching down <0.5 ns current pulse, whilst intrinsic infinite endurance is expected from the zero voltage stress applied during write operation.

There is still a major flaw. Fast switching of perpendicularly magnetized bit cells, a prerequisite for a scalable technology, requires a static in-plane magnetic field to break the symmetry between the magnetic up and down states. In other words, to achieve deterministic switching and not a never-ending magnetization precession, we are back to using external magnetic fields as in first-generation MRAM. Several alternative approaches to triggering field-less, fast switching in SOT have been proposed, yet none seems practical for product implementation.

There is still a strong appeal to explore SOT as there are potentially huge gains to be had. System-level simulations have shown that a significant decrease in chip size and power consumption can be expected in CPUs by replacing L2 and/or L3 SRAM cache by SOT. Not even to mention the possibility of normally-off/instant-on computing provided by the nonvolatility, nor the potential for execute-in-place functionality if RAM and ROM can be blended in a single memory block. Whether SOT can make it into the real world remains to be seen, but the prospects definitely make the journey worth the effort!