# Challenges for high performance and very low power operation at the end of the Roadmap

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Future ICs are facing dramatic challenges in performance, as well as static and dynamic power consumption, which could be overcome using disruptive concepts, device architectures, technologies and materials. Promising solutions includes III-V channels, heterojunctions, 2D layers, multi-gates structures, nanowires (NWs), tunnel FETs (TFETs), ferroelectric FETs (FE-FETs), and hybrid devices.

In the field of MOSFETs, several very interesting advances have been recently shown. Nanowire FET and 2D channels can improve sub-10 nm CMOS node performance and substantially reduce the supply voltage and short channel effects. In this respect, the bandgap of bilayer graphene and TMDs (e.g. $MoS_2$) can be controlled by the transverse electric field using a double-gate structure [1], while phosphorene is a 2D material with an intermediate bandgap, which could allow to obtain sub-5 nm gate length MOSFETs with very good control of short channel effects, high carrier mobility, and large $I_{ON}$ [2-4].

In the domain of small-slope switches, TFETs, FE-FETs and hybrid devices seem very promising. Thus far, no one has demonstrated a TFET that has simultaneously both a CMOS-competitive $I_{ON}$ and a sub-60 mV/decade subthreshold swing over several decades. But recently, a substantial improvement of TFET performance has been experimentally reported in a vertical InAs/GaAsSb/GaSb NW TFET [5], whereas very good simulated performance has been obtained for double-gate 2D TMD TFETs based on $WTe_2$ [6], $WTe_2/MoS_2$ heterojunctions [7], and van der Waals-bonded materials [8].

FinFETs using a ferrolectric gate ($Hf_{0.42}Zr_{0.58}O_2$), and therefore a negative capacitance, have recently experimentally exhibited a sub-60 mV slope, which could lead to larger driving current than TFETs [9]. Hybrid devices have also very recently demonstrated interesting properties, such as a swing of 4 mV/dec in phase-change TFET with a vanadium dioxide layer in the gate undergoing a metal-insulator transition under electrical excitation [10]. Another hybrid device based on a metal filament (Ag or Cu) formed at the drain of a Si MOSFET under sufficient applied bias, has led to a sharp subthreshold slope for several decades of drain current [11].

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