1D devices for Ge and 2D materials utilizing 3D integration technology

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Digital electronics is constrained by time delay as well as power and energy consumption. In a die, electrical energy is converted into heat at standby (static leakage current in MOSFET), during computation (switching of MOSFET devices) and upon data transport (switching of metal interconnects). Currently, as much as 50% of the dynamic power is consumed by switching the interconnects in a modern microprocessor. Since the on-die global metal wire length does not scale (due to *RC*-delay constraints), the preservation of today's IC architecture will cause an absolute predominance of interconnects on the overall power consumption, and make the systems totally energy inefficient. On the other hand, more and more researchers believe that device scaling will finally slow down. The challenge in the future is to increase the device density without scaling the device itself and develop more energy efficient ICs which are free from severe interconnect power consumption.

In this talk, we will discuss the advantage of 3D integration to increase the device density without scaling the devices, and shorten the interconnect length to reduce the power consumption. These 3D integrated transistors are of nanowire dimension and hence can be referred to as one-dimensional. Moreover, we will discuss novel photonic interconnects based on Ge and 2D layered materials (such as graphene and MoS_2) whose essential purpose is to provide low power consumption and high bandwidth.

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