Prospects and Challenges of Next Generation Memory Devices

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Since the first conceptualization of nonvolatile memory devices using floating gates in 1967, tremendous efforts have been made to develop high-density, low-cost, and nonvolatile solid-state storage devices for various applications. Among many kinds of nonvolatile memory devices, flash memories, which use an array of floating gate transistors to store information, are the most widely-used. During last decade, the memory density of NAND flash has been doubled in every year from 256 Mb to 64 Gb. Quite recently, Samsung Electronics and Toshiba announced that they are ready to ship NAND flash memories with 30-nm process technology. However, device scaling will reach definite limits within the next several years. Therefore, new and innovative design and technology are needed to increase the density of memory devices further, for example, novel device structures, manipulating current lithography tools, multilevel data storage, *etc*. Also, we need to think about the possibility of applications of many fascinating nanotechnology and nanostructured materials (for example, nanowires, nanotubes, nanoparticles, self-assembled materials and processes, nanopatterning techniques, *etc*.) to the next-generation memory devices.

In this presentation I will discuss in detail regarding the innovative technologies that make possible the device scaling up to 20-nm process technology, difficult challenges for memory devices beyond 20 nm feature size, and the technology gap between the top-down and bottom-up approaches for next-generation memory devices.