Silicon nanowire-based nonvolatile memory cells: Progress and prospects

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There is a widely recognized need for urgent progress in nonvolatile memory (NVM) technology, driven by the exponential market growth of the ubiquitous portable and mobile electronics, such as cell phones, music players, USB and memory cards, *etc*. Commensurate with this demand, intensive research is carried out around the world to improve present technologies and invent new ones: for example, no fewer than eight (out of a total of thirty one) technical sessions at the 2007 IEDM meeting and one out of three plenary talks at the 2008 IEDM meeting were dedicated on memory cell technology.

To enable continued scaling (Moore's law), NOR flash memory is been replaced (where possible) with the much denser NAND technology, but the industry consensus is that fundamentally new innovations must be introduced beyond the 45-nm lithography node generation [1]. One such innovation our research group and many others are pursuing is to design NVM cells based on silicon nanowires (SiNWs) [2]. There are several important reasons why SiNW NVM cells are outperforming conventional (planar) silicon NVM cells. First, because of the cylindrical symmetry, for the same value of the control gate voltage the electric field across the tunneling oxide is bigger than in comparable conventional cells, leading to either higher performance (faster program/erase), or to same performance at a lower power. Second, the cylindrical symmetry is particularly suitable for scaling NVM cells, where as short a channel length as possible is desired without reducing the gate oxide thickness too much, so that good retention is maintained. From the expression for the relevant "natural scaling length" λ_{CYL} [3],

$$\lambda_{CYL} = t_{Si}\sqrt{\frac{2\varepsilon_{Si}\ln(1+\frac{2t_{OX}}{t_{Si}})+\varepsilon_{OX}}{16\varepsilon_{OX}}}$$

it is clear that while λ_{CYL} (and thus channel length) scales down with t_{Si} (nanowire diameter), it only depends logarithmically on the tunneling oxide thickness t_{OX}.

We will present the theoretical background of the SiNW NVM cells, review the most relevant results from the literature, and discuss our latest results, including cell improvements by using various high-κ dielectric stacks. On the basis of this, an attempt will be made to project future progress and anticipate new innovations.

1. S. Lai, "Nonvolatile memory technologies: The quest for ever lower cost", *Tech. Digest IEDM* (2009), p. 11.
2. X. Zhu, Y. Yang, Q. Li, D. E. Ioannou, J. S. Suehle, and C. A. Richter, *Microelectronic Eng.* **85**, 2403 (2008).
3. C. P. Auth and J. D. Palmer, *IEEE Electron Dev. Lett.* **18**, 74 (1997).