Nanoelectronics era fabrication for a low-cost, portable, high-performance, low-energy-consuming and multifunctional electronics

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The microelectronics industry is facing historical challenges to down scale CMOS devices through the demand for low-voltage, low-power, high-performance and increased functionalities. The implementation of new materials and devices architectures will be necessary. High-κ gate dielectrics and metal gates are among the most strategic options to reduce power consumption and manage low supply voltage. Multigate, multichannel devices (Fig. 1) [1], sub 60mV/dec swing architectures [2], gate-all-around nanowires all can increase MOSFET current drive, reduce power at the L_G ~ 5 nm level, and allow new memory devices opportunities. By introducing new materials(Ge, III-Vs, carbon-based materials like diamond, graphene and CNTs, molecules, …), and new functions such as sensing and actuation (M/NEMS, filters, imagers, …), Si-based CMOS will be scaled beyond the ITRS as the system-on-chip/wafer platform (Fig. 2) [3]. The heterogeneous integration of these devices with CMOS will require new 3D and packaging schemes leading to an increase in effective packing density, functionality and improving systems figures of merit [4, 5].

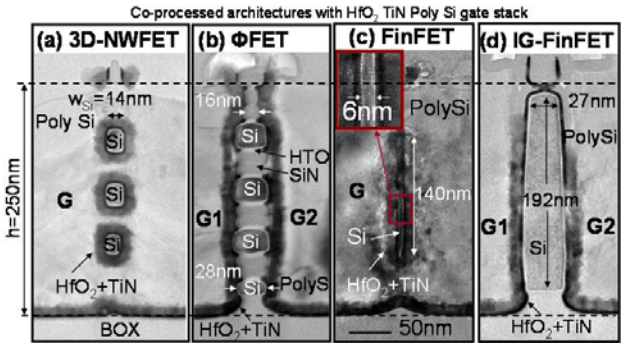

FIG 1. 3D-stacked Si nanowires for high density, high performance and low power consumption [1, 3].

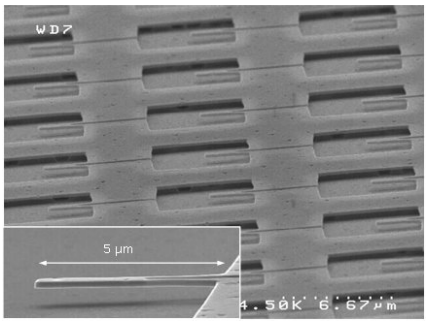

FIG. 2 CMOS compatible ultra-dense arrays (60,000/mm²) of NEMS-based cantilevers for ultra sensitive mass detection [3].

1. C. Dupré *et al.*, *Tech. Digest IEDM* (2008), pp. 748-751.
2. F. Mayer *et al.*, *Tech. Digest IEDM* (2008), pp. 163-166.
3. T. Ernst *et al.*, *Tech. Digest IEDM* (2008), pp. 745-748.
4. P. Batude, *Proc. ECS* (2008), VO 16, p. 47; *Proc. VLSI Symp*. (2009).
5. N. Sillon *et al.*, *Tech. Digest IEDM* (2008), pp. 595-597.