Silicon-based devices and materials for nanoscale CMOS and beyond-CMOS

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At the end of the ITRS, new materials, nanotechnologies and device architectures will be needed for nanoscale CMOS and beyond-CMOS. Silicon-on-insulator (SOI)-based devices are promising for the ultimate integration of electronic circuits on silicon [1]. We will discuss a number of key issues, including: the performance of single- and multi-gate thin film MOSFETs; the comparison between Si, Ge and III-V SOI channels; the effects of strain, high-κ materials, and Schottky source-drain (S/D) contacts. We then proceed to beyond-CMOS nanodevices based on nanowires or tunnel FETs and, finally, to an overview of advanced memory architectures on the nanoscale.

Strained SOI is very interesting for boosting performance, with electron and mobilities enhanced by uniaxial tensile and compressive strains respectively, down to ultrathin channels [2]. Schottky S/D engineering is also promising for nanoscale CMOS, with PtSi/Si contacts producing record current drive and RF performance in *p*-channel SOI MOSFETs [3]. In the high-κ arena, the product of κ and the energy barrier that determines the gate leakage current can be set lower for double-gate (DG) SOI than bulk CMOS, offering a wider choice of gate dielectrics [4]. Multi-gate architectures based on volume inversion are expected to provide higher current drive down to sub-10nm gate lengths [5]. Further out, multi-bridge-channel MOSFETs [6] and gate-all-around SOI nanowires with tunable thresholds [7] represent the ultimate integration of innovative nanodevices with promising electrical properties.

In the advanced memory arena, we will discuss capacitorless one-transistor DRAMs [8] and various variants of FinFlash memories that offer good downscaling prospects [9]. Independent DG FinFETs are also candidates for enhanced SRAM performance due to lower leakage and better noise margins [10]. Finally, there are promising tunneling FET candidates that may provide sharp switching for beyond-CMOS low-power applications, including DG high-κ TFETs, strain Ge DG with asymmetric source/drain and feedback TFETs [11–13].

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