Carbon-nanotube solutions for the post-CMOS-scaling world

Paul M. Solomon
IBM Research, Yorktown, U.S.A.

The CMOS research world has been up-ended in the past few years with the realization that the end of scaling is indeed approaching fast and that other, more radical solutions need to be found. Much work has been focused on investigating a radical (for CMOS) set of new geometries and materials, including strain engineering, 2D electrostatically confined structures, and 3D heterogeneous integration. These approaches extend the technology and provide a more powerful end-point, but do not drastically alter the scaling scenarios. The capabilities projected for future CMOS are enormously larger than even today's gigascale integrated product so the question arises as to the need for any CMOS follow-on at all. An interesting feature pertaining especially to the silicon-on-insulator approaches is that the "silicon" technology is becoming divorced from the bulk silicon material – indeed, for these technologies any convenient material could, in principle, be used for the substrate.

Of the various alternative "nano-offerings" investigated in the past few years, none can be seen as a serious competitor for this evolved CMOS. Device characteristics are poor, unreliable and noisy, and manufacturing methodologies are uncertain at best. A possible exception, at least in terms of the intrinsic device, is the carbon nanotube (CNT), and this will be the topic of my presentation. Carbon nanotubes can be thought of as perfect electron waveguides where electrons can by transported through unimaginably small channels without scattering off the boundaries. In addition phonon interactions are weak. This results in per-unit-channel-area properties vastly superior to silicon, with the additional advantage that these properties are symmetric for both *p* and *n* channel transport. Challenges to implementing this technology and realizing these intrinsic advantages in terms of system performance are formidable. Firstly, how do we place, or grow, CNTs of desired properties on the circuit substrate. Then, given such placement, how do we fabricate FETs with specific and tightly controlled characteristics, and with low parasitic capacitances and resistances. Last, but not least, how do we best use CNTs in circuits and systems, and what performance advantages are expected.

Two interesting application regimes are identified. Firstly in the low-power regime, the high intrinsic packing density and low intrinsic capacitance gives the CNT an advantage both in intrinsic and wiring capacitance. This could be further improved if metallic CNTS were used for the wires (taking the kinetic inductance into account). Secondly, their intrinsic high speed coupled with their ballistic properties open up the possibility of uses as discrete traveling wave-type amplifiers and oscillators up to the THz range.