Physical limits of Si CMOS: Real showstopper or wrong problem?

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From more than two decades technical papers announced the imminent dismissal of Si CMOS stressing the 1 µm barrier, then the 100 nm brick walls and recently the 10 nm limit: until now they all proved to be wrong. After analyzing the reasons of the failure of such claims we will look at the latest versions of the same theme, trying to outline the underlying assumptions of such assertions and possible shortcomings.

Assuming the "classical" Si CMOS will hit some limits in the future, the latest version of the ITRS roadmap gives a thorough analysis of possible candidates in this "Beyond CMOS" era. We will review the necessary criteria for a successful replacement of Si CMOS gate for information processing and make a critical assessment of such proposed devices.

However the question is: are we looking at the right problem? The focus on logic gates may just be the tree hiding the forest of issues to be addressed in information processing. We will also look at major pending problems like interconnecting those gates, making complex circuits manufacturable or even asking if any alternative information processing schemes may solve present hot topics in nanoelectronics.