

Tunneling Silicon-on-Insulator Transistors with Quantum Functionality

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Silicon-on-insulator (SOI) transistors built in thin fully-depleted Si channels on top of an insulating buried oxide are predicted by the various technology roadmaps to take over from bulk Si CMOS devices over the next few years. In the mainstream silicon technology, there is currently an ongoing debate about an appropriate double-gate SOI transistor geometry and fabrication sequence that will meet the architectural demands for end-of-roadmap Si devices. At the same time, the ongoing SOI miniaturization, with available Si channel and gate insulator thicknesses dropping to the nanoscale, is opening the door to quantum effect devices based on tunneling and/or charge quantization fabricated and integrable with mainstream CMOS. This is significant because it appears increasingly unlikely that any incompatible quantum-effect device architecture will make inroads against the rapidly evolving CMOS technology.

We have fabricated SOI transistor with an ultra-thin Si channel of ~ 5 nm, tunneling gate oxide of ~ 1 nm, and 100 nm gate length. In addition to good transistor characteristics, these same devices exhibit additional functionality at low temperature. The drain current I_D exhibits steps near the turn-on threshold voltage as a function of the backgate V_{BG} bias on the substrate. When operated as a gate controlled tunneling device, with source shorted to drain and I_G produced by tunneling from the gate to the channel, we observe structure in the $I_G(V_{BG})$ due to resonant tunneling into the quantized channel subbands. In the future, as SOI device fabrication advances, buried oxide thickness is reduced and Si channel uniformity is improved, the quantum effects will become stronger and appear at lower V_{BG} and higher temperature. This offers, at least in principle, the prospect of ULSI-compatible dual-use devices, with standard transistor operation or quantum functionality depending on the biasing.