NANOELECTRONIC TECHNOLOGY:
In Search of the Ultimate Device Structures

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OUTLINE

- INTRODUCTION
- EVOLUTION OF MOSFET STRUCTURES
- MAJOR ISSUES OF DEVICE SCALING
- NANOTECHNOLOGY OPTIONS AND ULTIMATE DEVICE
- CONCLUSION
SEMICONDUCTOR INDUSTRY: A KEY INDUSTRY FOR 21ST CENTURY

GLOBAL SALES ($Billions)

YEAR

1960 1990 2000 2010

ELECTRONICS
AUTOMOBILE
SEMICONDUCTOR
CAPITAL INVESTMENT IN SEMICONDUCTOR
## PROGRESS IN MICROELECTRONICS

<table>
<thead>
<tr>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Rule (μm)</td>
<td>25</td>
<td>0.09</td>
<td>270</td>
<td>↓</td>
</tr>
<tr>
<td>( V_{DD} ) (V)</td>
<td>5</td>
<td>1.2</td>
<td>4</td>
<td>↓</td>
</tr>
<tr>
<td>Wafer diameter (mm)</td>
<td>25</td>
<td>300</td>
<td>12</td>
<td>↑</td>
</tr>
<tr>
<td>Devices per chip</td>
<td>6</td>
<td>8( \times 10^9 )</td>
<td>10( ^9 )</td>
<td>↑</td>
</tr>
<tr>
<td>DRAM density (bit)</td>
<td>–</td>
<td>1k</td>
<td>4G</td>
<td>4( \times 10^6 )</td>
</tr>
<tr>
<td>Nonvolatile memory density (bit)</td>
<td>–</td>
<td>2k</td>
<td>2G</td>
<td>10( ^6 )</td>
</tr>
<tr>
<td>Microprocessor clock rate (Hz)</td>
<td>–</td>
<td>750k</td>
<td>3G</td>
<td>4( \times 10^4 )</td>
</tr>
<tr>
<td>Transistor shipped / year</td>
<td>(10^7)</td>
<td>(10^{18})</td>
<td>(10^{11})</td>
<td>↑</td>
</tr>
<tr>
<td>Average transistor price ($)</td>
<td>10</td>
<td>(2\times10^{-7})</td>
<td>(5\times10^{-7})</td>
<td>↓</td>
</tr>
</tbody>
</table>
ITANIUM MICROPROCESSOR
( 410 Million Transistors  374 mm²  0.13µm  1.5 GHz )
CPU MHz Trend

10 GHz CPU by 2007

MHz


10,000 1,000 100

8080 8086 286 386™ CPU 486™ CPU Pentium® CPU Pentium® II CPU Pentium® III CPU Pentium® 4 CPU
MOORE’S LAW

YEAR


DRAM DENSITY

10^4 10^5 10^6 10^7 10^8 10^9 10^10 10^11 10^12

64Gb 0.05 μm
16Gb 0.09 μm
4Gb 0.13 μm
1Gb 0.18 μm
256Mb 0.25 μm
64Mb 0.35 μm
16Mb 0.5 μm
4Mb 0.7 μm
1Mb 1.0 μm
256kb 1.4 μm
64kb 2.0 μm
MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor)
FIRST COMMERCIAL MOSFET, 1964
Fairchild Data Sheet for p-Channel MOSFETs

Preliminary Specifications — October 1964

FI 100
P-CHANNEL MOS FIELD-EFFECT TRANSISTOR
DIFFUSED SILICON PLANAR DEVICE

The FJ100 is a semiconductor device with a high voltage (less than 100V) and low current (less than 10A) designed for use in DC power supplies. It has a high thermal stability, making it suitable for operation in high temperature environments. The FJ100 is a vertical-type device, which allows for higher power densities and lower parasitic capacitance compared to horizontal types. Its high-voltage capability makes it ideal for high-voltage applications such as DC power supplies and converters. The FJ100 is available in a range of case styles, including plastic and ceramic packages, which are designed to provide maximum reliability and performance.

Physical Dimensions

The physical dimensions of the FJ100 are as follows:

- Width: 5.2 mm
- Height: 5.2 mm
- Length: 5.2 mm

Handling Instructions

When handling the FJ100, it is important to avoid static discharge, which can damage the device. Ensure that all handling tools are properly grounded. The FJ100 is sensitive to static discharge, so take necessary precautions to avoid static damage. Always use proper anti-static bags and devices to protect the FJ100 from static discharge. When operating the FJ100, ensure that it is properly populated on the circuit board. The FJ100 should be soldered using a low-heat soldering iron to avoid damaging the device. Always use a proper anti-static mat and workstation to handle the FJ100 safely.
Planar CMOS Transistor Scaling

Today

Future

50 nm
30 nm
20 nm
15 nm

Gate Length
14 nm Gate Length CMOS
(IEDM’2002, S.27.1, p.639)
Evolution of Device Structure

- Ideal sub-threshold slope (~ 60 mV/dec at room temperature)
- High current drive
- Low off current
- Good short-channel effect control
- Non-sensitive to parameter fluctuation
6 nm Gate Length UTB SOI PMOS

(IEEDM’2002, S.10.6, p.267)
Issues for UTB SOI CMOS

- SCE control \( T_{SOI} \approx 1/3L_{min} \)
- Parasitic S/D resistance
- Quantum confinement effect
  - \( V_{th} \) increase
- Body thickness fluctuation
  - \( V_{th} \) increase
  - Mobility degradation
Quasi-planar SOI FinFET

Advantages
- Relaxed constraint on channel thickness
- Relaxed constraint on EOT
- Improved SCE control
- Compatible with modern manufacturing steps

Issues
- Formation and control of fine Si fins
- Formation and control of sidewall spacer
- Parasitic S/D resistance
- Vth adjustment
10 nm Gate Length FinFET
(IEDM’2002, S.10.2, p.251)
10 nm Gate Length FinFET
(IEDM’2002, S.10.2, p.251)
Major Issues for Device Scaling

• **Leakage Currents**
  - Tunneling currents from gate to channel, body to drain, and source to drain
  - Thermally generated subthreshold channel current

• **Fluctuation effects**
  - Line edge roughness
  - Film thickness control (channel and gate dielectric)
  - Dopant distribution

• **Power Consumption**
MOSFET EFFECTIVE DIELECTRIC THICKNESS

![Graph showing the trend of gate oxide thickness from 1970 to 2010. The x-axis represents the years, and the y-axis represents the gate oxide thickness in nanometers. The graph shows a decreasing trend.]
Fluctuation Effects

Line width

Dopant concentration

Film Thickness

Poly-Si Gate

SiO₂

UTB SOI

SiO₂
Power Density Will Get Even Worse

(Andrew S. Grove, Luncheon Talk in IEDM’02)
Nanoelectronic Devices Options

Which can replace Si CMOS?

Targets:
- Lower cost
- Less power consumption
- Higher performance

Carbon Nanotube (CNT)
Molecular Devices
Single electron transistor (SET)
Spintronics
DNA IC
Requirements for Nanotechnology Options

- Feature size < 10 nm
- High energy conversion efficiency
- High speed
- Room temperature operation
- Good stability, uniformity and reliability
NANOTECHNOLOGY OPTIONS

- Carbon-nanotube FET
  - difficulty of forming low resistance contact
  - difficulty in forming nanotubes with the desired physical features
  - how to position nanotubes in a given position in a cost-effective way

- Molecular Devices
  - limitation in operating temperature
  - difficulty in making contact to individual molecules

- Quantum-dot Cellular Automata (Single-electron Parametron)
  - limitation in operating temperatures
  - sensitivity to random background charge
  - slow speed
  - difficulty in transmitting signals across larger intra-die distances
The Ultimate MOS Transistor
(Y. Taur, in short course program of IEDM’01)

4 nm thick undoped Si

High-k dielectric with EOT = 0.5 nm

Self-aligned metal gates with tunable work functions for threshold control

Tapered source-drain fan-out for reduction of electrical and thermal resistance without high overlap capacitance

(ITRS’2001, 2016, 25 nm-node, physical gate length for MPU: 9 nm)
MEMORY DENSITY OF DRAM AND SET

- 256T
- 64T
- 16T
- 4T
- 1T
- 300K
- NOVORAM
- SET-FET HYBRID
- 40K
- 10K
- FET DRAM (SIA Forecast)
- 256G
- 64G
- 16G
- 4G
- 1G

Minimum Feature Size (mm)
# APPLICATIONS AT THE SCALING LIMIT

<table>
<thead>
<tr>
<th>Application</th>
<th>Memory (GB)</th>
<th>Comp. Rate (GIPS)</th>
<th>Power / DSP (W)</th>
<th>Si Area (cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speech recognition (to text)</td>
<td>0.01-0.1</td>
<td>0.1-1</td>
<td>0.001</td>
<td>0.1</td>
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<tr>
<td>Real time language translation</td>
<td>0.1</td>
<td>1-10</td>
<td>0.01</td>
<td>0.2</td>
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<tr>
<td>Video encoding, very high res.</td>
<td>0.01</td>
<td>20-200</td>
<td>0.2</td>
<td>0.6</td>
</tr>
<tr>
<td>(1920 ×1200, 30 fps)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2-way video wrist watch</td>
<td>0.01</td>
<td>0.05</td>
<td>0.0002</td>
<td>0.01</td>
</tr>
<tr>
<td>PDA</td>
<td>0.1</td>
<td>1-10</td>
<td>0.01</td>
<td>0.2</td>
</tr>
<tr>
<td>Factoring 512 bit numbers</td>
<td>1</td>
<td>4000</td>
<td>10</td>
<td>40</td>
</tr>
<tr>
<td>Deep Blue chess</td>
<td>3</td>
<td>10000</td>
<td>3</td>
<td>100</td>
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<tr>
<td>QM-based device simulation¹</td>
<td>10</td>
<td>100</td>
<td>30</td>
<td>16</td>
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<tr>
<td>PetaFLOPS computing challenges²</td>
<td>(3 \times 10^4)</td>
<td>(10^6)</td>
<td>(10^6)</td>
<td>(5 \times 10^4)</td>
</tr>
</tbody>
</table>

¹ Power based on general-purpose processor applications instead of DSP
CONCLUSION

• Major issues for device scaling are leakage currents, fluctuation effects, and power consumption.

• The double-gate SOI MOSFET is a promising candidate for the ultimate device structure, its gate length can be scaled down to 10 nm.

• There are numerous applications of MOSFET at the scaling limit (around 2015), and silicon technology is expected to continue as the most powerful driver of the Information Age.