**Extreme CMOS Devices in Future Using SOI Technology**

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We have proposed the device design strategy for ultimate CMOS devices with ultra-low power and high performance in the sub-10nm regime. The device is in the form of semi-planar SOI MOSFET with three-dimensional gate structure. Good examples are the triangular wire channel MOSFET and FinFET with a small aspect ratio. In these devices, the short channel effect is well suppressed while the sufficient body effect is maintained in order to suppress the fluctuations of device characteristics. Moreover, the quantum effects and single electron charging effects that appear in the nanoscale device are positively utilized for the mobility enhancement, threshold voltage control, and the suppression of fluctuations. In this talk, I will demonstrate the validity of this device concept by showing our experimental data and simulation results.