Gate Coupling and Double-Gate Operation in Nanometer Thick SOI MOSFETs

J. Prétet, A. Ohata, S. Cristoloveanu, C. Aydin, A. Zaslavsky, D. Mariolle, and S. Deleonibus
IMEP and *CEA–LETI, Grenoble, France, Gunma Univ., Japan, Brown University, USA*

There is no doubt that ultimate MOSFET scaling, beyond 10–20 nm channel length, will require ultra-thin fully-depleted (FD) silicon-on-insulator (SOI) transistors with double-gate (DG) architecture. Simulations show the perfect electrostatic control in DG MOSFETs and their superior scalability. On the experimental side, despite much effort to devise a practical DG process flow, quantifying DG *vs*. SG operation has not been easy. Some DG geometries cannot be operated in SG mode, whereas comparing devices fabricated with different technologies is also debatable because material and processing issues can interfere with the purely physical mechanisms. There are two open questions:

- Are the classical mechanisms and models for FD MOSFETs still valid below 10 nm thickness, where the coupling between the two interfaces is exacerbated, and quantum confinement occurs?
- What is the real advantage of DG over SG MOSFETs and how can it be measured?

In this work, we revisit the coupling effects in the context of ultra-thin channels and show the influence of low-temperature operation. We also examine the accurate biasing for a reliable comparison of SG and DG modes. The usual procedure is to operate the same transistor either in SG mode (with the back gate grounded) or in DG mode. Virtual DG operation is achieved by adjusting the front and back gate biases to account for existing asymmetries (different thickness and/or work function of gate oxide and buried oxide):

$$V_{G2} - V_{T2} = (t_{OX2}/t_{OX1})[V_{G1} - V_{T1}] \quad (1)$$

We will demonstrate that this biasing rule should be used with extreme care. For example, in weak inversion it leads to extravagant subthreshold slopes far below 60 mV/decade at 300 K. Since $V_{T1,2}$ vary with opposite bias, what are the proper values to be used? In general, $V_{T1,2}$ are taken from measurements performed with the opposite gate grounded. This inaccuracy, which has escaped attention for years, will be illustrated by experiments.

Virtual DG operation actually means that when one gate reaches inversion, the other gate should be in inversion too. The procedure we propose consists in superimposing on the same graph the variations of the front- and back-channel threshold voltage with the opposite gate bias $V_{T1,2}$ ($V_{G2,1}$). In a relatively thick transistor, the two curves intersect and provide the accurate $V_{T1,2}$ values to be inserted in Eq. (1). But the case of the 5 nm thick MOSFET is more challenging because the two curves *coincide* and no intersection can be defined. We argue that any point on this common curve provides acceptable (V_{T1}, V_{T2}) biasing for DG operation.

This revised DG operation was used to compare the transconductance in DG and SG modes. A gain of 200% is the natural consequence of using two gates. In our case, additional gain is observed, presumably due to the increase in mobility in volume inversion regime. This optimistic scenario, supported by our data, is an interesting issue for further debate.