Strategies at the end of CMOS scaling

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After more than three decades of uninterrupted exponential growth, the silicon VLSI technology is approaching device limits which are dictated by device physics. The limits are well known and involve increasingly compromising off-state currents for higher on-state performance. Other semiconductor materials do not appear to fundamentally change this outlook, and none seem at this point to offer a rationale for switching from silicon. While it is commonly assumed, with justification, that silicon systems will continue with rapid improvements long after scaling at the device level has stopped, nevertheless, any "end of the road" device improvements will have a permanent future legacy.

In this talk I will assume that technology will continue to improve even beyond the point where it is capable of producing the "ultimate" scaled device, and consider device geometries, topologies and circuit configurations best able to exploit this situation, with the goal of continued improvements in circuit performance and power reduction.