Self-evolving neuromorphic networks based on nanoscale latching synapses

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Future VLSI implementation of bio-scale neuromorphic networks requires nanoscale synaptic devices. Indeed, in order to place a network with 10^{10} neurons with connectivity 10^4, on a 10×10 cm^2 chip, the synapse should fit onto a 10x10 nm^2 area. Such density may be achieved using single-electron devices [1] based on the "Coulomb blockade" effect.

We have designed [2] a single-electron device which may serve as a BiWAS (binary-weight, analog-signal) synaptic node bridging two nanowires. It consists of 3 islands: one working as a single-electron transistor, and two others forming a single-electron trap, with the trap island capacitively coupled to the transistor island. If voltage V between the wires is low, the trap in equilibrium has no trapped electrons, leaving the transistor in the Coulomb blockade state. If V is increased beyond a certain threshold, one electron is injected into the trap. In this charge state the Coulomb blockade in the transistor is suppressed, keeping the wires connected at any V. However, if the node activity (voltage V) is low for a long time, the electron tunnels out of the trap and the transistor closes, disconnecting the wires.

We have carried out [2] a preliminary study of two promising architectures of adaptive ("plastic") networks based on 2D square arrays of the single-electron synaptic nodes. In one architecture, axon and dendrite trees grow spontaneously on the array, stimulated by activity of randomly located neural cell bodies. The forming patterns are strikingly similar to those observed in bio networks. However this architecture scales unfavorably at high connectivity, although it may still be useful for some systems, e.g., artificial retinas.

This drawback is avoided in another, "randomized distributed crossbar" architecture in which each cell is hard-wired to a subset of other cells, with the binary synaptic weights controlling which of the connections are currently active. This network scales much better, actively using virtually all the chip area. As a result, bio-scale systems may be implemented on a single chip with 1-nm-scale nanofabrication technologies (presently under active development in several laboratories). Speed scaling of this network is also very impressive: the estimated time of cell-to-cell data transfer may be as short as 100 ps, at least 7 orders of magnitude faster than in bio systems. This implies that one global evolution iteration (apparently equivalent to one biological generation) may be achieved in just a few seconds.

At the meeting, I will present results of synaptic node modeling, simulated behavior of network fragments (with up to 10^6 synapses), and the future prospects of work in this direction.

[1] K. Likharev, Proc. of IEEE **87,** 606 (1999).

[2] S. Fölling, Ö. Türel, and K. Likharev, “Self-evolving neuromorphic networks with single-electron switching latches as synaptic nodes”, submitted for presentation at the ECCTD’01 meeting (Helsinki, Finland, August 28-31,2001).