Gate dielectrics for deep sub-0.1 μm CMOS

Hiroshi Iwai and Shun-ichiro Ohmi
Tokyo Institute of Technology, Japan

Recent rapid progress of information technology owes very much to that of semiconductor technologies, especially to that of CMOS. However, the downsizing of CMOS devices is now facing severe difficulties for sub-0.1 μm generations because of various expected limitations. For, example, SiO_2 has been used almost exclusively as the material for the gate insulator since the first realization of the MOSFET in 1960. Recently, thinning of the gate oxide has proceeded very aggressively and the gate SiO_2 film thickness has already plunged into the direct-tunneling regime and reached 2 nm in the product level. Now, further thinning of the gate SiO_2 dielectrics is reaching its limits and the development of new gate dielectrics is becoming the most critical issue for the next generations of CMOS circuitry.

In this paper, current problems of the ultra-thin gate dielectrics are discussed from the different viewpoints of various LSI applications. In order to overcome the problems, introduction of new materials and device structures have been seriously investigated. In this paper, we present preliminary results of studies on future gate dielectrics for deep-sub-0.1μm CMOS, such as ultra-thin direct-tunneling SiO_2 and new high-κ dielectric materials.