The MOS transistor will be deservedly sanctified, but not before completing the terminal stages of its heroic evolution. At present, shrinking the transistor length is the driving force down the SIA roadmap, with scheduled milestones and little room for artistic variations. We expect the silicon-on-insulator (SOI) transistor to be a leading competitor, although it still needs to secure widespread sponsorship and an enthusiastic audience.

In regard to ordinary downscaling, it is frequently omitted that a small geometry also implies chopping the width. As refined isolation schemes are being developed, we will enjoy novel edge effects, including lateral quantization. We will show that, in very narrow channels, the carrier lifetime is degraded and the floating body effects tend to vanish. We will then demonstrate that, in an SOI MOSFET, the reduction of the length and width is highly facilitated if the channel thickness is reduced too. As a result of this type of miniaturization, the device physicist needs to continue his education: forget about short-length effects, skip the small-area effects, and just think in terms of small-volume effects.

According to other forecasts, the SOI transistor will undergo genetic modifications, infusing new functionality into extremely thin channels. Tiny quantum-effect devices, such as single-electron or tunnelling devices, are already born, in vitro. A different approach is to graft a second gate or a ground plane onto a regular SOI MOSFET, in order for the transistor to run faster, perhaps fly, while still saving energy. More or less technologically viable, albeit admirably sophisticated, grafting techniques for double-gate transistors will be described. A key difficulty is the fabrication of self-aligned double gates in a realistic fashion. However, our simulations indicate that misalignment of the two gates may not be a critical issue as long as one gate is slightly longer. In these devices, interesting coupling effects arise, causing exotic transconductance curves.