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Abstract

The charge injection transistor or CHINT is a semiconductor device based on real-space transfer of hot electrons between two conducting layers, separated by a potential barrier. Recently, a significant progress has been achieved at Bell Laboratories in the implementation of CHINT devices. Using InGaAs/InAlAs heterostructure materials and novel epitaxial contacts, nearly ideal characteristics were obtained, e.g. an NDR with a peak-to-valley ratio approaching 10^4 at room temperature and a transconductance $g_m > 20$ S/mm. The nature of hot-electron injection in CHINT allows the implementation of novel circuit elements. In particular, we have proposed and demonstrated a multiterminal single-device structure that works as a functional element with three symmetric logic inputs X_1, X_2, X_3 and one output equal to $(X_1 \cap X_2 \cap X_3) \cup (\bar{X}_1 \cap \bar{X}_2 \cap \bar{X}_3)$. This device, called the NORAND, can perform both as a NOR (X_1, X_2) and as an AND (X_1, X_2) element, reprogrammable electrically by changing the X_3 input. The NORAND element permits the implementation of circuits in which the function of a particular logic element is not fixed by the layout but is reprogrammable in the course of the circuit operation.

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TECHNICAL MEMORANDUM

ABSTRACT

The charge injection transistor or CHINT is a semiconductor device based on real-space transfer of hot electrons between two conducting layers, separated by a potential barrier. Recently, a significant progress has been achieved at Bell Laboratories in the implementation of CHINT devices. Using InGaAs/InAlAs heterostructure materials and novel epitaxial contacts, nearly ideal characteristics were obtained, e.g. an NDR with a peak-to-valley ratio approaching 10^4 at room temperature and a transconductance $g_m > 20\,S/mm$. The nature of hot-electron injection in CHINT allows the implementation of novel circuit elements. In particular, we have proposed and demonstrated a multiterminal single-device structure that works as a functional element with three symmetric logic inputs X_1, X_2, X_3 and one output equal to $(X_1 \cap X_2 \cap X_3) \cup (\bar{X}_1 \cap \bar{X}_2 \cap \bar{X}_3)$. This device, called the NORAND, can perform both as a $NOR\,(X_1, X_2)$ and as an $AND\,(X_1, X_2)$ element, reprogrammable electrically by changing the X_3 input. The NORAND element permits the implementation of circuits in which the function of a particular logic element is not fixed by the layout but is reprogrammable in the course of the circuit operation.

1. INTRODUCTION

The charge-injection transistor (CHINT) or negative resistance field-effect transistor (NERFET) are two modes of operation of a three-terminal heterostructure device [1-3] based on the real-space transfer of hot electrons between. The concept of real-space-transfer (RST) [4] describes the process in which electrons in a narrow semiconductor layer, accelerated by an electric field parallel to the layer, acquire high average energy (become "hot") and then spill over an energy barrier into the adjacent layers. Even though only a small fraction of electrons, those in the high-energy tails of the hot-carrier distribution function, can participate in this process, those tails are replenished at a fast rate corresponding to the energy relaxation time, mainly owing to electron-electron collisions. Typically, multiple collisions result in a Gaussian distribution of carrier velocities, which can be interpreted by analogy with the Maxwellian ensemble, but with an effective electron temperature T_e. The injection process can be viewed in analogy to the usual thermionic emission, and for high T_e it can be very efficient.

The original idea of employing the RST in devices was to induce a negative differential resistance (NDR) in multilayered heterostructures [4-5], an effect discovered experimentally [6] and studied in great detail [7]. Transistor applications of the RST began with the proposal [1] of a three-terminal structure where hot-electron injection occurs between two conducting layers isolated by a potential barrier and contacted separately. This structure is schematically illustrated in Fig. 1. One of the two layers ("emitter") has source and drain contacts and plays the role of a hot-electron cathode. The other layer ("collector") is separated by a potential barrier. When the emitter electrons are heated by the source-drain field most of them do not reach the drain but are injected over the barrier into the collector layer; a strong negative differential resistance (NDR) develops in the drain circuit. The transistor action results from an efficient control of the electron temperature T_e and hence the injection current I_C by the input voltage V_D.

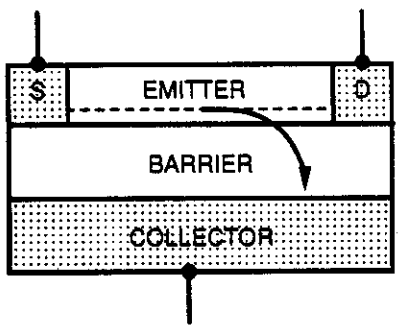

Figure 1: Schematic diagram of a charge injection transistor. The arrow shows the direction of electron flow.

A number of functional applications have been contemplated [8-11], based on the unique characteristics of three-terminal RST devices. Recently, the scope of such applications was expanded by the invention [12] of a new multiterminal device structure, called the NORAND. The principle of NORAND embodies the basic symmetry inherent in the charge injection by RST: direction of the collector current is the same irrespective of the polarity of the heating voltage, i.e. it does not matter which of the surface electrodes plays the role of the source and which of the drain. The operation of

NORAND has been demonstrated experimentally and will be discussed in this paper (Sect. 4). This discussion will be preceded by a review of the recent progress in the implementation of charge injection transistors.

In recent years, charge injection transistors have been extensively investigated, both experimentally [13-20] and theoretically [21-26]. The early experimental studies were based on GaAs/AlGaAs heterostructures. This work has been reviewed in Refs. [11] and [26]. More recently, there have been reports of the implementation of RST transistors in strained-layer InGaAs/AlGaAs heterostructures grown on GaAs substrates [15-17]. In most of these structures, the RST is likely to be accompanied by a momentum-space transfer, which limits the intrinsic performance of CHINT/NERFET devices. Monte Carlo simulations [25] have shown that formation of Gunn domains lowers the NDR peak-to-valley ratio and limits the ultimate device speed. It is of considerable interest, therefore, to implement these devices in materials where the momentum-space transfer would be absent or negligible relative to the RST. Working in this direction, several groups have recently realized three-terminal RST devices, based on the injection of hot holes across a potential discontinuity in the valence band of GaAs/AlGaAs [18] and GeSi/Si [19] heterojunctions.

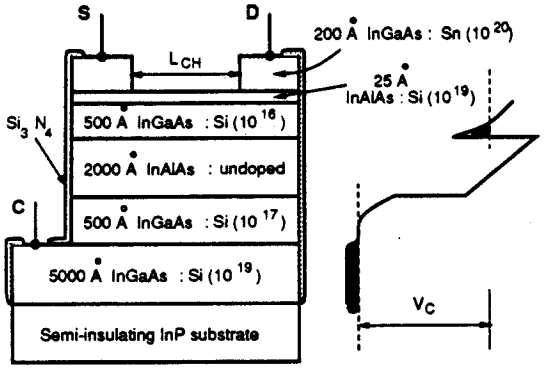

Figure 2: Cross-section of the device structure and the energy-band diagram under an applied collector bias [14]. The trench in the heavily Sn-doped cap layer defines the emitter channel.

Another attractive material combination is the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ system lattice-matched to InP. Advantages of this system for RST transistors stem from the low effective electron mass $m = 0.042\,m_0$ in the Γ valley of InGaAs, the high conduction-band discontinuity ($\Delta E_C \approx 0.5$ eV), and the still higher satellite-valley separation ($\Delta E_{\Gamma L} \approx 0.55$ eV) [27]. One can expect that if the effective barrier height for charge injection (which is less than ΔE_C) is lower than $\Delta E_{\Gamma L}$, then the RST should have a lower threshold than the momentum-space transfer. The relatively large ΔE_C (compared to $GaAs/Al_xGa_{1-x}As$ for $x \leq 0.4$) allows one to expect a lower leakage current of "cold" electrons and, hence, an improved performance at room temperature. The lower effective mass favors the efficiency of electron heating in an electric field. Although these advantages were apparent long time ago [2], they had not been exploited until recently because of the difficulties in implementing non-shorting ohmic contacts. Previous attempts at implementation of CHINT/NERFET in this system were not successful: the usual Au-Ge alloyed contacts to the channel either showed non-ohmic behavior [9], or, if alloyed at an elevated temperature, penetrated too deep, resulting in an electrical short to the collector. This essential problem was solved recently [13] by using an epitaxially-grown cap layer, heavily doped with tin, which is subsequently patterned lithographically to form the source and drain n^+ contacts.

2. DEVICE STRUCTURE

The structure described below was reported in Ref. [14]; it represents an improvement in several respects over the earlier study [13]. Figure 2 shows a cross section of the device obtained after several wet chemical etching and ion milling steps. The heterostructure has been grown by molecular beam epitaxy at 550 C on a semi-insulating iron-doped InP (100) substrate. It consists of the following layer sequence: a 5000 A-thick n^+ $In_{0.53}Ga_{0.47}As$ collector layer followed by a 500 A-thick lightly doped n^- $In_{0.53}Ga_{0.47}As$ setback layer, a 2000 A-thick undoped $In_{0.52}Al_{0.48}As$ barrier layer, and a lightly doped 500 A-thick $In_{0.53}Ga_{0.47}As$ emitter layer, followed by a 25 A-thick n^+ $In_{0.52}Al_{0.48}As$ etch-stop layer, and an ultra-heavily doped (Sn) 200 A-thick $In_{0.53}Ga_{0.47}As$ cap layer.

The active area of the device represents a strip of the emitter layer whose dimension along the line connecting the source and drain is 9.5 μm and the width W varies from 25 μm to 75 μm. All patterns were defined by the standard optical contact lithography, including the critical definition of a trench separating the source and drain areas. This trench, 200 A-deep, defines the emitter channel. It is obtained by a highly selective wet chemical etching of $In_{0.53}Ga_{0.47}As$, which stops reliably at a 25 A-thick $In_{0.52}Al_{0.48}As$ layer introduced specially for that purpose. For different devices, the trench length L_{ch} varied from 0.6 μm to 5 μm. After the etching, the exposed portion of the channel is entirely depleted by the surface potential, but with a positive voltage applied to the collector, a two-dimensional electron gas is induced in the channel, as illustrated in Fig. 2.

Contacts to the channel were ohmic down to liquid helium temperatures. We found no degradation of the contacts from the introduction of the 25 A-thick InAlAs etch-stop layer.

An important element in the structure is the lightly-doped setback layer between the barrier and the collector. Its purpose is to reduce the possibility of an unintentional doping of the barrier during growth by an out-diffusion of donors from the collector. Compared to structures without the setback layer [13] the dielectric strength of the barrier is substantially enhanced.

3. STATIC CHARACTERISTICS

Figure 3 describes the current-voltage characteristics of a 25 μm wide 1 μm long CHINT/NERFET device at $T = 300$ K. The striking feature is a NDR in the drain characteristic with a peak-to valley (PTV) ratio typically exceeding 1000 at room temperature. In contrast to most of the previous studies of the device, this strong NDR is obtained in the presence of a low leakage current due to "cold electrons". We see that the NERFET switches almost the entire source current from the drain branch of the biasing circuit to the collector branch. The resulting collector current I_C is more than twice larger than the peak value of I_D.

As the inset to Fig. 3 shows, both the leakage current and the PTV ratio are increasing functions of the collector voltage. At $V_C = 4.4$ V, the observed PTV exceeds 7000. Our measure of the leakage is the value of I_D at $V_D = 0$; in a perfectly symmetric device it equals half the value of I_C at the same bias. Within the limit of V_C imposed by a dielectric breakdown of the $In_{0.52}Al_{0.48}As$ layer, we observed no tendency toward saturation in either PTV or $I_D(0)$. The dielectric strength of the barrier and its abruptness at the collector side is evidenced by the low leakage at $V_D = 0$ and also by the broad valley in I_D at high drain biases. As seen in Fig. 3, this valley persists up to $V_D - V_C \approx 5$ V, until it is overwhelmed by an injection of "cold electrons" from the collector.

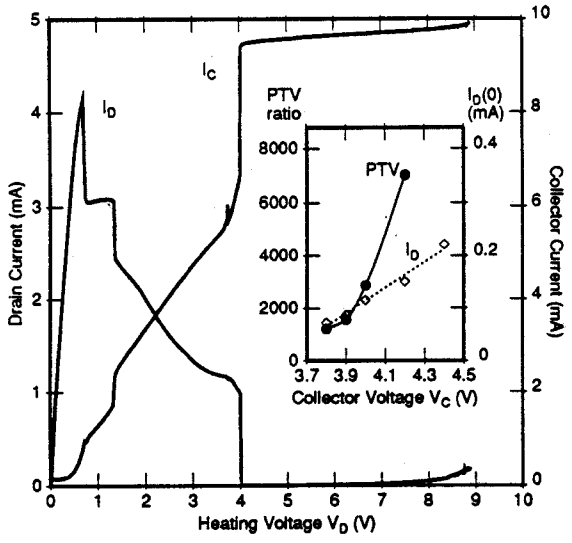

Figure 3: Room temperature characteristics [14] of a device with $W = 25$ μm and $L_{ch} = 1$ μm. The drain current (I_D) and collector current (I_C) are plotted versus the heating drain voltage V_D at a fixed collector bias $V_C = 3.9$ V. Insert shows the collector-bias dependence of the peak-to-valley ratio and the leakage current, defined as the magnitude of I_D at $V_D = 0$.

The variation of V_C affects not only the PTV ratio but also the critical voltage, V_{NDR}, for the onset of NDR. At high collector voltages the V_{NDR} shifts to lower values. It is likely that this shift is due to the increased importance of the tunneling process in the RST [21]. At high V_C, the charge injection occurs via "thermally" assisted tunneling. This is equivalent to an effective lowering of the barrier height; a given RST current is therefore realized at a lower electron temperature, and hence at a lower V_D.

Because the electron temperature in the channel is controlled by the drain field that at a fixed V_D increases with decreasing L_{ch}, the V_{NDR} shifts to lower values for shorter shannel lengths [14]. In devices with $L_{ch} = 0.6$ μm, the onset of the NDR is observed at drain voltages as low as 0.34 V. Note that this V_{NDR} includes the voltage drop in the contacts but still is appreciably lower than the barrier height $\Delta E_C/e \approx 0.5$ V. This provides an evidence that the RST proceeds from the tails of a "thermalized" hot-electron distribution function rather than by a single-event scattering of ballistically accelerated electrons.

A fundamentally interesting question is: what limits the real space transfer in CHINT/NERFET structures? Figure 3 clearly indicates that if we were able to apply higher collector bias without a breakdown of the barrier the PTV ratio would increase even further. At the same time, for a given V_C both the valley and the injection currents reach relatively flat plateau values as a function of the heating voltage. This fact indicates a breakdown of the electron temperature approximation. Indeed, for a given T_e the RST process depletes the channel exponentially with the distance toward the drain – without a limit [8]. Since with increasing V_D the high-field region expands like it does in a field-effect transistor (as the pinch-off point moves toward the source), theories based on the electron temperature approximation [21] predict an exponential decrease of I_D with increasing heating voltage.

Monte Carlo studies [24,25] have shown that in GaAs/AlGaAs devices the RST process is limited by a momentum-space transfer of hot electrons into the satellite valleys, that cuts off the heating of channel electrons. It is unlikely, however, that momentum-space transfer effects could play a significant role when the satellite-valley separation is much higher than the effective barrier height. We believe that such is the situation in our present devices, at least at high V_C. In the absence of momentum-space transfer, the RST process can be *self-limited*, when the electron concentration n in the channel drops below a certain critical value n_{cr} that itself is a function of the barrier height and therefore of V_C. As the data in Fig. 3 indicate, the drain current at the valley is below 1 mA/cm. This corresponds to $n \lesssim 10^9$ cm^{-2}. At such low carrier concentrations, the electron temperature approximation can be expected to break down [26].

Indeed, a T_e different from the lattice temperature T is established when the electron-electron scattering time is substantially shorter than the relaxation time associated with the lattice. At low electron concentrations, the high-energy portion of the energy distribution that is constantly depleted by the RST, is no longer efficiently refilled and can be strongly depressed compared to a

Maxwellian curve. Although the total distortion of the distribution function is "integrally" weak, because it affects only the tails of the distribution containing a small fraction of electrons, in those very tails the distortion can be quite strong [28]. This means that one can expect a self limitation of the RST process with the channel concentration never dropping below a critical level – determined, for a given collector barrier height, by the concentration dependence of the electron-electron interaction.

The importance of interelectronic interactions and cooperative effects in CHINT cannot be overemphasized, although at present our description of these processes is at best qualitative. Such effects are likely to be crucial for a quantitative understanding of the phenomenon of ultra-high transconductance, discussed below.

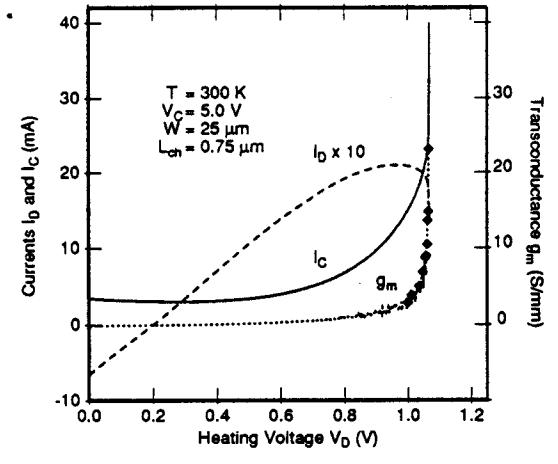

Figure 4: Drain current, I_D, collector current I_C, and the transconductance g_m as functions of the drain voltage at a high collector bias V_C=5.0 V [14]. Large enhancement in the transconductance is observed at $V_D > V_{NDR}$ in the stable NDR region. Diamonds represent the actual discrete data points for g_m in that region obtained by a numerical differentiation of the I_C curve.

The transconductance, g_m is an important figure of merit for any transistor. For the CHINT, it is defined as the slope of the $I_C(V_D)$ characteristic per unit width W of the emitter channel: $g_m \equiv W^{-1}\partial I_C/\partial V_D$ at a constant V_C. In GaAs/AlGaAs CHINT the highest reported [11] transconductance was $g_m \approx 1{,}000$ mS/mm. The transconductance characteristics of our present devices are shown in Fig. 4, which plots the V_D dependence of I_D, I_C, and g_m at a fixed collector bias V_C = 5.0 V. We see that in a narrow range of V_D above 1 V the injection current rises by an order of magnitude, leading to an extremely high g_m = 23.1 S/mm. When the injection current exceeded certain limit (≈50 mA for 25 μm devices), the InAlAs barriers usually suffered a dielectric breakdown. Therefore, we had to limit the I_C: the data presented in Fig. 3 were collected with a compliance set at 40 mA. The large boost in the injection current is observed within a range V_D = 1.02 – 1.03 V right after V_{NDR}, but before the onset of circuit oscillations caused by the NDR. The existence of a stable NDR region has been observed only at large values of V_C.

The ultra-high transconductance appears to be related to the formation of a high-field RST domain in the channel. We believe that at high values of V_C the domain formation occurs continuously as a function of V_D. In a narrow range of V_D, corresponding to the stable NDR, the source-to-drain electric field (initially, relatively uniform over the channel because of the high carrier concentration) concentrates in a "hot spot" (the domain) depleted of carriers. A small variation of V_D reduces the domain size, thus producing a large change in the electric field, hence a large variation in the electron temperature and the injection current that gives rise to a high g_m.

Although the idea of a continuously shrinking domain is highly speculative, we stress that some sort of a cooperative process is likely to be required in order to explain the observed ultra-high values of g_m. Our understanding in terms of a global charge redistribution in the device is supported by Monte Carlo studies of CHINT/NERFET [25]. The measured characteristics in the narrow range of ultra-high g_m are highly reproducible with no sign of hysteresis.

4. CHARGE INJECTION LOGIC

The fact that the RST current I_C does not depend on which of the two surface terminals, *S* or *D*, is chosen to be the source, allows the implementation of devices in which the role of a particular terminal in the circuit is not defined by the layout.

Consider the circuit illustrated in the top portion of Fig. 5 not as a transistor but as a logic element with inputs **S** and **D** corresponding to the biases on the *S* and *D* electrodes, respectively. The point to note is that the logic function **OUT**(**S**, **D**) represents an exclusive NOR, since **OUT** is high when I_C is low (no RST) and **OUT** is low when the injection current is flowing. The latter situation results only when the voltages **S** and **D** are sufficiently different.

The bottom part of figure 5 illustrates a schematic diagram of the proposed logic element NORAND which has three logic inputs $\mathbf{X}_j$ (j = 1, 2, 3) and one output **OUT**. Which of the $\mathbf{X}_j$ will serve as a source and which as a drain is determined only at the time when a particular logic operation is performed. The value of **OUT** is high (logic 1) is only when all three $\mathbf{X}_j$'s have same value (high or low). All the other six possible logic input configurations lead to the same high injection current resulting from hot electron emitters formed in two of the three channels, X_{3-1}, X_{1-2}, and X_{2-3}. Three of these configurations correspond to the presence of two sources and one drain, the other three to one source and two drains.

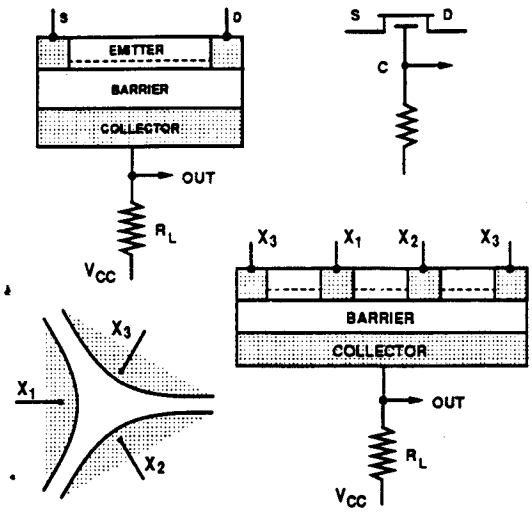

Figure 5: Schematic illustration of the charge injection logic. Top figure on the right introduces a circuit symbol of the CHINT. The bottom figures illustrate the NORAND element. Figure on the bottom left describes a symmetric arrangement of three identical channels, X_{3-1}, X_{1-2}, and X_{2-3}. By symmetry, one has the same amount of hot-electron injection for any of the six states of binary input in which at least one of the three X_j's is different from the other two. The bottom figure describes an asymmetric NORAND layout. One of the electrodes is physically (but not logically) split, resulting in a "periodic" boundary condition, equivalent to the three-fold rotational symmetry of the left figure.

It is easy to see that the logic function OUT($\{X_j\}$) is given by

$$(X_1 \cap X_2 \cap X_3) \cup (\bar{X}_1 \cap \bar{X}_2 \cap \bar{X}_3),$$

where the symbols $\cap$, $\cup$, and $\bar{A}$ stand for logic functions **AND**, **OR**, and **NOT A**, respectively. The truth table of the NORAND is as follows:

	I		II		III		IV	
X_1:	0	0	1	1	0	0	1	1
X_2:	0	1	0	1	0	1	0	1
X_3:	0	0	0	0	1	1	1	1
OUT:	1	0	0	0	0	0	0	1
	$\overline{X_1 \cup X_2}$ (NOR)				$X_1 \cap X_2$ (AND)			

We see that the NORAND operates as a NOR(X_1, X_2) when the input to X_3 is *low*, and as an AND(X_1, X_2) when X_3 is *high*. It is clear that the three-fold symmetry of the device ensures that the injection current has the same value in all the six states corresponding to logic OUT=0. Of course, one can achieve a similar effect without an exact three-fold symmetry, e.g. with a "cylindrically" symmetric arrangement of the $\{X_j\}$ electrodes, as illustrated in the bottom right part of Fig. 5.

The operation of NORAND has been demonstrated [12] with a circuit consisting of three discrete CHINT devices with similar characteristics. The circuit, shown in the insert to Fig. 6, is functionally equivalent to a monolithic with three input terminals. In this experiment we used the devices described in Ref. [13], as the improved structure of Fig. 2 had not yet been available. The common-source characteristics of one these devices are shown in Fig. 6. For the load device we took a transistor used as a nearly constant current source, see the dotted line in Fig. 6.

The reason we had to use a high-impedance load is instructive. For a meaningful demonstration the device should, of course, operate with a logic gain. In switching a single device, the gain equals $\bar{g}_m R_L$, where R_L is the load resistance and $\bar{g}_m$ However, because of the unavoidable slight differences between the devices it was inconvenient to operate within the narrow range of high g_m. Another, more critical, difficulty was associated with the fact that each emitting channel, X_{i-j}, $i, j = 1, 2, 3$, should, ideally, be stable against oscillations in the input circuit, i.e., the logic state corresponding to a *high* value of $|X_i - X_j|$ should be outside the NDR region of the $I_D(V_D)$ characteristic. Experimentally, at high V_C the NDR region typically spans about 1.5 to 3.5 V, cf. Fig. 3. This feature is undesirable because it implies that in order to obtain a voltage gain, one would have to use a high load resistance. However, the wide extent of the unstable region appears to be related to the interaction between the active device and the reactive impedances of an external circuit. The NDR region becomes narrower for devices with smaller channel widths.

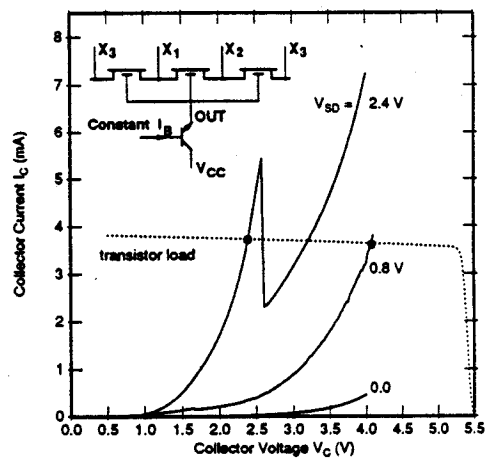

Figure 6: Common-source characteristics of one of the devices forming a composite NORAND element [12]. Collector current I_C is plotted against the collector voltage V_C with the heating voltage V_D as a parameter. Dotted line indicates the load curve for a transistor load used in the demonstration. The circuit connection is shown schematically in the insert.

For the purpose of illustration, we ensured the circuit stability by performing the switch in a range of relatively low average transconductance $\bar{g}_m$ and employing a high-impedance load. The measured functional characteristics of the circuit showed logic gain in reproducing the NORAND truth table. These characteristics are illustrated in Fig. 7. The two traces on the left correspond to $X_3 = 0$ and illustrate the operation of $\mathbf{NOR}(X_1, X_2)$; the traces on the right correspond to $X_3 = 4\,V$ and the operation of $\mathbf{AND}(X_1, X_2)$. The order of traces agrees with that in the truth table: e.g., the bottom trace on the right illustrates the last two columns of the table.

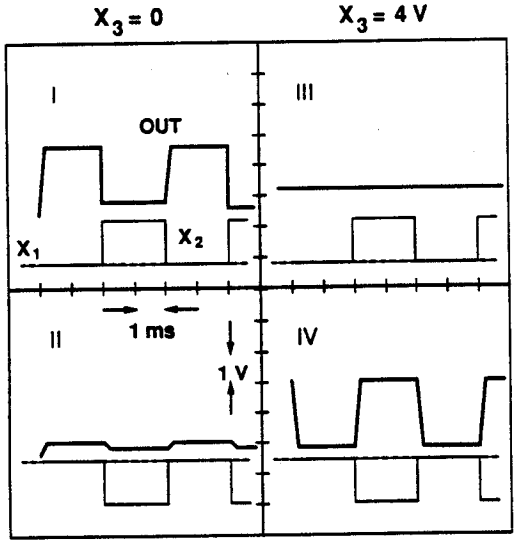

Figure 7: Experimental illustration of the operation of a NORAND element assembled from three discrete CHINT devices with similar characteristics (as in Fig. 6): oscilloscope traces of the NORAND response function. Dashed lines correspond to X_1, thin solid lines to X_2, and heavy lines to OUT. Traces I and II were obtained with $X_3 = 0$; traces III and IV correspond to $X_3 = 4\,V$. Each quadrant in the figure illustrates two columns of the NORAND truth table with the roman numerals corresponding to those in the table. All traces refer to an origin at the bottom left corner in each of the four quadrants.

In order that a logic device could be used in integrated circuits, it is necessary that its input and output voltages be consistent. As Fig. 7 suggests, in the case of NORAND this may require an additional level-shifting circuitry. In principle, this would not be a necessary requirement if only the NOR part of the NORAND truth table were to be employed. In the NOR configuration, the device has a well-defined ground level, and a consistent range of input-output characteristics can be found, as we have ascertained experimentally. On the other hand, in the AND configuration the low-OUT voltage must be higher than the lowest of the input voltages. In an optimized device, this difference can be made small, but since it would still accumulate after several stages, the level shifting will be mandatory. Further discussion of this interesting point will be made elsewhere in the context of a specific application. Of course, it is well-known that all logic functions can be implemented on the basis of a NOR element alone.

The NORAND functional element departs radically from all previously contemplated uses for multiterminal RST devices [26]. At the same time, it represents a natural embodiment of the essence of hot-electron injection by the RST. Compared to all existing logic families, the NORAND offers a considerable economy in the layout of basic functional elements. Moreover, it promises faster operation of these elements, since the entire function is implemented within one gate delay of a high-speed transistor.

5. MICROWAVE STUDIES OF CHINT

High-frequency characterization has been reported for CHINT devices implemented in GaAs/AlGaAs heterostructures [10] and, recently, for a novel three-terminal RST device in a strained-layer InGaAs/AlGaAs/GaAs heterostructure [17]. Microwave studies of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ transistors have just began with the preliminary results reported in Ref. [20]. In these studies, the CHINT devices of the variety described in Sect. 2 were characterized on-wafer at room temperature in a frequency range 0.5–25.5 GHz. The small-signal current gain (h_{21}) and power gain parameters (MAG/MSG) were calculated from the measured scattering S-parameters and plotted against frequency for a number of DC biasing conditions.

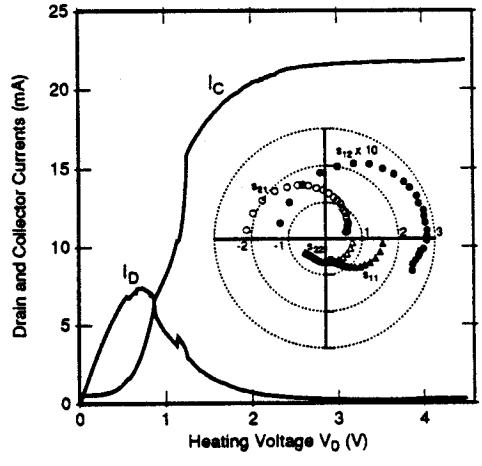

Figure 8: Static *I-V* characteristics at $V_C = 4.0\,V$ and the scattering parameters measured for the same device at $V_C = 4.0\,V$ and $V_D = 0.8\,V$. Device geometry: $W = 25\,\mu m$, $L_{ch} = 0.8\,\mu m$. The S-matrix data are plotted in the complex plane for frequencies ranging from 0.5 to 25.5 GHz. After Ref. [20].

Figure 8 displays both the static characteristics and the S-parameter data for the same device. The static measurement was obtained prior to microwave testing using low-inductance probes. The low-inductance probes substantially reduce the circuit oscillations at low frequencies caused by the NDR in the drain circuit. The microwave data presented in Fig. 8 correspond to a region immediately following the onset of NDR in the drain characteristic. Compared to bipolar or field-effect transistors, the scattering parameters of CHINT show several unusual features. In particular, $\arg(S_{12}) \rightarrow \pi$ in the DC limit, which may indicate the existence of a positive feedback. Also, the magnitude of the input reflection coefficient $|S_{11}|$ can be larger than unity due to the NDR in the input circuit. On the other hand, the behavior of S_{21} and S_{22} shows no apparent anomalies.

The calculated small-signal current gain, h_{21}, and the maximum available gain (MAG) are plotted in Fig. 9 for the same DC bias as in Fig. 8. In the range of frequencies where Rollet's factor K is less than unity, the maximum stable gain (MSG) was calculated instead of MAG. At these frequencies, the device is potentially unstable. Since in the range where MAG exists ($K>1$) it equals $MSG \times [K-(K^2-1)^{1/2}]$, the composite MSG/MAG curves exhibit a kink near $K=1$. For some bias conditions, the device is unstable up to the highest measured frequencies and the corresponding curves exhibit no kink [20].

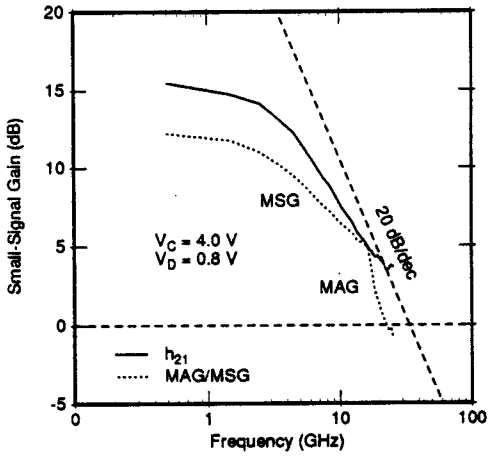

Figure 9: Small-signal gain parameters calculated from the S-parameters displayed in Fig. 8.

In general, the high-frequency roll-off of the gain parameters in our device had a slope smaller than 20 dB/decade. Extrapolating at 20 dB/decade we found that the highest unity-current-gain frequency is slightly above 40 GHz. The maximum oscillation frequency, f_{max}, is difficult to obtain for bias points where MAG does not exist within the measurement range, i.e. if $K < 1$ for $f \leq 25.5$ GHz. However, for some DC bias conditions, e.g. at $V_D = 1.10$ V and $V_C = 4.5$ V, the device still oscillates ($K = 0.68$) at $f = 25$ GHz. Extrapolating from the frequency dependence of the K-factor, we found that $K \rightarrow 1$ at $f \approx 35$ GHz, which gives an estimate for the f_{max} in our device. The measured gain cutoff frequencies exceeded ~20 GHz in a range of V_D at least 0.5 V wide and a still wider range of V_C.

The charge injection transistor is attractive for high speed electronics since its ultimate performance is believed to be limited only by the time of flight of hot electrons across the barrier layer (another delay associated with the time required for the electron scattering to establish an effective temperature in the emitter channel is expected to be shorter than 1 ps). For our present device with a 2000 Å thick barrier the transit time can be estimated to be between 2 and 3 ps. This would mean an f_T between 50 and 80 GHz. Inasmuch as the bandwidth of our devices is below this fundamental limitation, it is likely that the RC delay associated with the parasitic drain-to-collector capacitance is still responsible for limiting the device speed, just as it was the case for devices used in earlier microwave studies [10].

One obvious avenue for improvement is to minimize the drain area. However, since the transit time decreases while the RC delay increases with diminishing barrier thickness, the drain-to-collector capacitance will always remain a factor to be concerned about. A promising direction is to use for the barrier layer semiconductors like InP where the electronic transport is faster. An interesting alternative approach was recently reported by Hueschen et al. [17]. These authors studied an RST transistor, very similar in concept to CHINT, but with an inverted structure in which the collector is the top layer. This allows to reduce the drain-collector capacitance, which has probably contributed to the higher current-gain cutoff frequency (f_T = 60 GHz) found in ref. [17].

6. CONCLUSION

We have reviewed recent progress in the implementation and characterization of charge injection transistors as well as their possible use in logic circuits. It is clear that the InGaAs/InAlAs heterostructure lattice-matched to InP is an excellent material system for the implementation of real-space transfer transistors. However, the use of InP itself for the barrier layer is expected to yield improvements in microwave performance.

Static characteristics of InGaAs/InAlAs CHINT/NERFET devices are quite striking, with the peak-to-valley ratio in the NDR exceeding 7,000 and the CHINT transconductance reaching 20 S/mm. Studies of charge injection in these devices are expected to bring forth new information about the physics of hot-electron transport in heterostructures. It is clear that future research on charge injection transistors must be focussed on their intended applications. Perhaps the most interesting recent accomplishment related to CHINT is the proposal and experimental demonstration of a new logic element, called the NORAND. The demonstrated fact that the NORAND can perform both AND and NOR functions, reprogrammable with the characteristic CHINT speed in the course of computation, represents unique property of charge injection by real-space transfer.

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Attachments
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