Real-space transfer in three-terminal InGaAs/InAlAs/InGaAs heterostructure devices

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Three-terminal real-space transfer devices have been implemented in InGaAs/InAlAs/InGaAs heterostructure material. The use of nonalloyed contacts provides excellent ohmic contacts to the channel without compromising insulation from the second conducting layer. The observed negative differential resistance has a peak-to-valley ratio that typically exceeds 100, both at room temperature and cryogenic temperatures. The highest observed peak-to-valley ratio at 300 K was 490. With increasing heating voltage, the injection current across the InAlAs barrier rises in a sequence of sharp steps. We explain this feature by an instability caused by a positive feedback between the heating field in the channel and the local real-space transfer current.

Charge-injection transistor (CHINT) or negative resistance field-effect tansistor (NERFET) is a three-terminal semiconductor device based on the effect of real-space transfer (RST) of hot electrons between conducting layers, separated by a potential barrier and contacted independently.[1–4] One of these layers, referred to as the channel, has two surface contacts, source and drain. Application of a source-to-drain bias leads to a heating of channel electrons and charge injection into the second conducting layer. The channel acts as a hot-electron *emitter* and the second conducting layer as a *collector*. The device shows a strong, negative differential resistance (NDR) in the source-drain characteristic (the NERFET action[2]), and an efficient control of the injection current by the drain voltage (CHINT action[3]). Such devices have been extensively investigated, both experimentally[5–8] and theoretically.[9,10] Successful experimental studies, reported so far, used GaAs/AlGaAs heterostructures,[2–7] and strained-layer InGaAs/InAlAs heterostructures grown on GaAs substrates.[8] In most of these structures, the RST is likely to be accompanied by a momentum-space transfer, which limits the intrinsic performance of CHINT/NERFET devices. Monte Cario simulations[10] suggest that formation of Gunn domains degrades the NDR and limits the ultimate device speed. It is of considerable interest, therefore, to implement these devices in materials where the momentum-space transfer would be absent or negligible relative to the RST. Working in this direction, we have recently realized devices, based on the injection of hot holes across a potential barrier in the $Ge_{0.2}Si_{0.8}$/Si valence band.[11]

Another attractive material combination is the InGaAs/InAlAs system lattice matched to InP. Because the separation $\Delta E_{\Gamma L}$ between the Γ and the lowest satellite valleys in the conduction band of InGaAs seems to be higher[12] than the conduction-band discontinuity[13] $\Delta E_C \approx 0.5$ eV between InGaAs and InAlAs, the RST may have a lower threshold than the momentum-space transfer (it is unlikely, however, that the latter can be fully suppressed.). The relatively large ΔE_C (compared to GaAs/$Al_xGa_{1-x}As$ for $x \leqslant 0.4$) allows one to expect a lower leakage current of "cold" electrons and, hence, an improved performance at room temperature. A further advantage of the InGaAs/InAlAs system results from the lower electron effective mass in InGaAs, which favors heating effects in an electric field. Previous attempts at implementation of CHINT/NERFET in this system[3] were not successful; a major difficulty was associated with Au-Ge alloyed contacts to the channel. These contacts either showed nonohmic behavior, or, if alloyed at an elevated temperature, penetrated too deep, shorting electrically to the collector. In the present work, this essential problem was solved by using an epitaxially grown cap layer, heavily doped with tin and subsequently patterned lithographically to form the source and drain n^+ contacts.

The structure was grown by molecular beam epitaxy (MBE) at 550 °C on a semi-insulating iron-doped InP (100) substrate. The sequence of epitaxially grown layers was as follows: first a 5000-Å-thick $In_{0.53}Ga_{0.47}As$ collector layer with a donor (Si) concentration of $N_D = 10^{19}$ cm^{-3}, next a 2000-Å-thick undoped $In_{0.52}Al_{0.48}As$ barrier layer, followed by a 500-Å-thick $In_{0.53}Ga_{0.47}As$ channel layer, lightly doped with Si ($N_D = 1 \times 10^{16}$ cm^{-3}), and a 300-Å-thick $In_{0.53}Ga_{0.47}As$ cap layer, heavily doped with Sn ($N_D = 1 \times 10^{20}$ cm^{-3}). Figure 1 shows a cross section of the device structure obtained after several etching steps in H_3PO_4:H_2O_2:H_2O. All patterns were defined by a standard optical contact lithography, including the critical definition of the trench between source and drain areas. This trench, approximately 300 Å deep, removes the n^+ cap layer from the top of the channel. The emitter length, defined by the trench, varied from 0.6 to 1.2 μm for different devices. The emitter width varied from 25 to 75 μm. After the etching, the exposed portion of the channel is entirely depleted by the surface potential. Therefore, the channel conduction relies on a positive collector voltage, which induces an inversion layer as illustrated in Fig. 1. Epitaxial contacts to the channel were ohmic in our experiments down to liquid-helium temperatures—without any high-temperature alloying.

The use of nonalloyed contacts produced a dramatic enhancement of the NERFET performance. NDR characteristics with peak-to-valley ratios of over 100 are routinely observed in our devices both at room and cryogenic temperatures (see Figs. 2 and 3).[14] The highest observed peak-to-valley ratio at room temperature was 490, the current I_D switching from 4.83 mA to 9.86 μA in a 25 μm channel-width device.

Figure 2 presents the drain I_D and the collector I_C cur-

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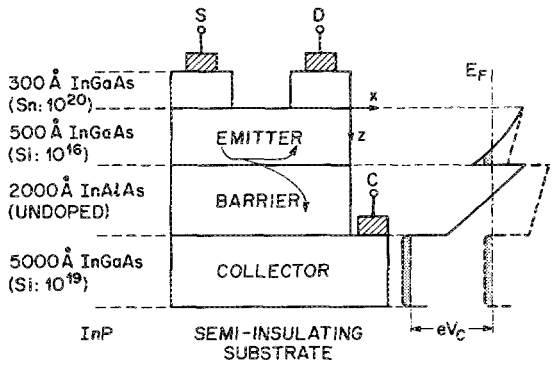

FIG. 1. (a) Cross section of the device structure and (b) the energy-band diagrams in the emitter portion of the channel. The equilibrium diagram is shown by a dashed line and diagram under an applied collector bias by a solid line. Arrows indicate the directions of electron flow when both the drain and the collector are biased.

rent characteristics at room and liquid-nitrogen temperatures. The characteristics are plotted versus the drain voltage for different fixed biases on the collector, viz., $V_C = 1.0$, 2.0, and 3.0 V. At low drain voltages, below the onset of NDR at $V_D \approx 0.7$ V, we observe typical field-effect transistor source-drain characteristics, accompanied by a gradual increase in I_C due to the RST of hot carriers. In this range the weak RST does not significantly affect the drain current. At $V_D = 0.72$ V, the RST increases in a step-like fashion and the drain current drops precipitously. Note that the drop in I_D is larger than the jump in I_C, which implies a drop in the source current. At $V_D = 2.4$ V (for $T = 77$ K) or $V_D = 2.2$ V (for $T = 300$ K) a second abrupt drop in the drain current is observed together with a jump in the collector current. Beyond this point, we observe a nearly flat valley in I_D and a plateau in I_C. These plateaux persist over a broad range of V_D, until the injection of cold electrons from the collector to the drain takes over at $V_D > V_C$. It is noteworthy that the peak-to-valley ratio in Fig. 2 is actually higher at 300 K than

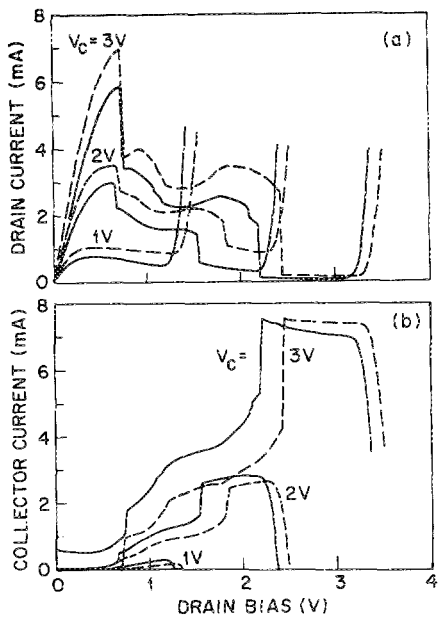

FIG. 2. Basic device characteristics: (a) Drain current vs the drain voltage at 300 K (solid lines) and 77 K (dashed lines). Curves are labeled by the value $V_C = 1$, 2, and 3 V. (b) Corresponding plots of the collector current vs the drain voltage.

at 77 K. This observation is common to all present devices and is likely to be related to a parasitic leakage of cold electrons from the drain area to the collector.

The two steps described above have been seen in all working devices for all available emitter widths and lengths. Exact position on the V_D axis, where these steps occur, varied from one device to another and with the temperature, but qualitatively they remained similar in the whole range $4.2 \lesssim T \lesssim 300$ K. The first step, corresponding to the onset of NDR, moves slightly to lower drain voltages with lowering T, as can be expected from the reduction in phonon scattering, but its position is almost insensitive to the collector voltage. The second step typically moves toward higher drain voltages with increasing V_C. This step occurs typically at lower V_D in devices with smaller channel widths.

The behavior in between the main steps is not universal, even with the sign of the resistance being positive in some devices and negative in others. The shape of the characteristic in this region can be varied by changing the RC constant of the external circuit. Many devices exhibited more than two steps in the drain and the collector characteristics. Figure 3 shows exemplary characteristics of such a device. The displayed curves correspond to 6.5 K, but a similar multiple-step structure was present also at room temperature. In all cases, the total source current, $I_S = I_D + I_C$, plotted in Fig. 3(c), drops abruptly, together with the drain current at the onset of the NDR (here at $V_D = 0.68$ V) and rises abruptly, similarly to the collector current, at the onset of the final plateau ($V_D = 2.2$ V). In the intermediate region, abrupt but small drops of I_S are observed, and in some cases steps in I_C and I_D nearly cancel each other. As a function of V_C these steps behave similar to the second main step, moving toward higher drain voltages. The NDR and the ladder structure in the I-V characterstics require a certain minimum collector voltage. For the device of Fig. 2, no steps are observed below $V_C \approx 1.5$ V. Above this threshold, the step height is an increasing function of the collector voltage. In some devices, the number of intermediate steps increases with V_C.

Steps in I-V characteristics are, generally, indicative of a positive feedback loop that causes the system to switch. Let

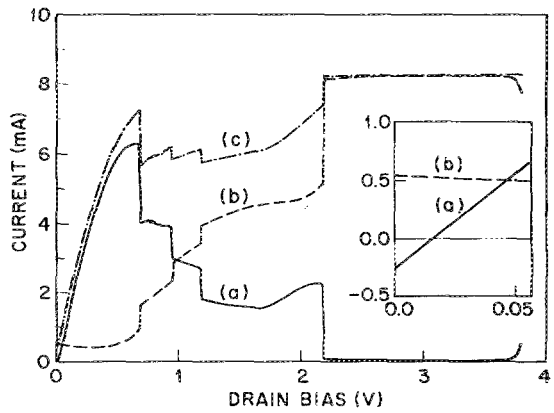

FIG. 3. (a) Drain, (b) collector, and (c) source currents vs the drain voltage at the collector bias $V_C = 3.5$ V and the temperature $T = 6.5$ K. Multiple steps in the I-V characteristics are clearly in evidence. At $V_D = 0.67$ V the total (source) current abruptly drops, whereas at $V_D = 2.2$ V it rises. The peak-to-valley ratio in the plot (a) is 210. Inset shows the characteristic at low V_D in expanded scale. Parasitic source-to-collector leakage at the valley is of the order of 100 μA.

us discuss its possible physical mechanism. As the drain voltage is increased from zero, the RST process begins in some section of the emitter channel, where the electric field is largest. We shall refer to this section as the "hot spot". At the onset of charge injection, the voltage difference between the collector and the hot spot begins to diminish. This reduces the electron density at the hot spot, which in turn increases its resistance and causes a larger fraction of the source-to-drain voltage to drop across the hot spot region. The increased lateral electric field raises the electron temperature and the hot spot becomes even hotter. This self-accelerating instability[15] leads to an avalanche-like increase in the RST from the emitter hot spot and the emergence of a high-field domain in the emitter. The process is limited by a negative feedback, arising with the decrease of the electric field in the InAlAs barrier near the interface with the InGaAs channel at the hot spot and the drop in I_S due to the lowering of the electric field in the section between the source and the hot spot. (The latter mechanism explains the abrupt drops in I_S evident in Fig. 3, that accompany steps in I_D.) It is clear that the hot spot potential Φ_H cannot rise above V_D because that would be prevented by diffusion of cold electrons from the drain. If $V_D > V_C$ then the process will stabilize as Φ_H approaches V_C, since the diminishing field in the barrier will effectively raise the space-charge accumulation of injected electrons dynamically stored during the transit across the barrier. One can expect a strong suppression of the RST if the interface field becomes negative; the steady state is probably established before that happens.

After the RST is stabilized and a high-field domain established, a further increase of V_D may initiate a new avalanche RST process and a new domain in the channel, leading to multiple steps in the I-V characteristic, as in Fig. 3. The last step seems to be different in that it is accompanied by an abrupt *rise* in the source current. It is clear that as V_D increases, the domain cannot stay in the vicinity of the drain, where the electric field across the barrier diminishes and can even reverse its direction. We believe that the last step at high V_D may be associated with the hot spot moving toward the source, raising the electric field there and thereby increasing the source current.

Our present experimental data are insufficient to discuss what limits the lateral domain size and whether these domains can propagate, as in the Gunn effect. These interesting questions warrant further studies, combined with a numerical simulation of the device. Another important question is: what is responsible for the saturation of the collector and drain current in the final plateau region? Similar saturation is normally seen in GaAs/AlGaAs devices, where it has been attributed[10] to the effect of the momentum-space transfer which cuts off the heating to channel electrons. This process can also take place in our devices, especially at lower collector voltages. As the V_C increases, the barrier becomes transparent for high-energy electrons that tunnel under the top of the barrier. This "thermally assisted" hot-electron tunneling process plays an important role in the operation of CHINT.[9] It is unlikely that momentum-space transfer effects could play a significant role when the satellite-valley separation is much higher than the effective barrier height. As discussed in Ref. 16 the self-limitation of the RST may result when the electron density in the domain becomes so low that the high-energy tails of the electron distribution function above the barrier height are not repopulated by the electron-electron scattering.[17]

In conclusion, we reported experimental results on hot-electron injection in CHINT/NERFET devices implemented in a InGaAs/InAlAs/InGaAs heterostructure lattice matched to InP. The use of nonalloyed epitaxial contacts and excellent properties of the InGaAs/InAlAs system produced a dramatic improvement of the device characteristics and brought into focus a peculiar instability of RST process. A plausible mechanism of this instability is related to a positive feedback between the RST and the heating electric field in the emitting channel. This feedback leads to the formation of high-field domains in the emitter channel.

[1] A. Kastalsky and S. Luryi, IEEE Electron Device Lett. **EDL-4**, 334 (1983).

[2] A. Kastalsky, S. Luryi, A. C. Gossard, and R. Hendel, IEEE Electron Device Lett. **EDL-5**, 57 (1984).

[3] S. Luryi, A. Kastalsky, A. C. Gossard, and R. Hendel, IEEE Trans. Electron Devices **ED-31**, 832 (1984).

[4] S. Luryi and A. Kastalsky, Superlatt. Microstruct. **1**, 389 (1985).

[5] A. Kastalsky, J. H. Abeles, R. H. Bhat, W. K. Chan, and M. Koza, Appl. Phys. Lett. **48**, 71 (1986).

[6] A. Kastalsky, R. Bhat, W. K. Chan, and M. Koza, Solid-State Electron. **29**, 1073 (1986).

[7] T. K. Higman, S. J. Manion, I. C. Kizilyalli, K. Hess, and J. J. Coleman, Phys. Rev. B **36**, 9381 (1987).

[8] M. E. Favaro, G. E. Fernandez, T. K. Higman, P. K. York, L. M. Miller, and J. J. Coleman, J. Appl. Phys. **65**, 378 (1989).

[9] A. A. Grinberg, A. Kastalsky, and S. Luryi, IEEE Trans. Electron Devices **ED-34**, 409 (1987).

[10] I. C. Kizillyalli and K. Hess, J. Appl. Phys. **65**, 2005 (1989).

[11] P. M. Mensz, S. Luryi, J. C. Bean, and C. J. Buescher, Appl. Phys. Lett. **56**, 25 June (1990).

[12] One estimate of $\Delta E_{\Gamma L} = 0.71$ eV in $In_{0.53}Ga_{0.47}As$ can be obtained by a linear interpolation between the values of $\Delta E_{\Gamma L} = 0.31$ and 1.16 eV for GaAs and InAs, respectively; see Table IX in J. R. Chelikowsky and M. L. Cohen, Phys. Rev. B **14**, 556 (1976). Photoemission studies [K. Y. Cheng, A. Y. Cho, S. B. Christman, T. P. Pearsall, and J. E. Rowe, Appl. Phys. Lett. **40**, 423 (1982)] suggest a smaller value $\Delta E_{\Gamma L} = 0.55$ eV at 300 K.

[13] R. People, K. Wecht, K. Alavi, and A. Y. Cho, Appl. Phys. Lett. **43**, 118 (1983).

[14] In general, the source-drain characteristic of a NERFET can be affected by a parasitic leakage of cold electrons to the collector layer, especially at high V_C. In particular, it affects the peak-to-valley ratio, as is clearly seen in Fig. 2(a), where this ratio is *higher* at room temperature than at 77 K. At collector voltages producing highest peak-to-valley ratios, the data of Refs. 6 and 8 show a leakage comparable to the peak drain current. Thus, the peak-to-valley ratio of 160, reported in Ref. 6, is achieved at $V_C = 8$ V, where the leakage current is around 2 mA. In our present devices, the maximum leakage at $V_C = 3.5$ V is only of order 100 μA.

[15] A meaningful analogy can be drawn between this process and the current-driven instability which can occur in a single-barrier heterostructure diode, cf. K. Hess, T. K. Higman, M. A. Emanuel, and J. J. Coleman, J. Appl. Phys. **60**, 3775 (1986).

[16] S. Luryi, in *Heterojunction Band Discontinuities: Physics and Device Applications*, edited by F. Capasso and G. Margaritondo (Elsevier, Amsterdam, 1987), Chap. 12, pp. 533–535.

[17] This effect is similar to the distortion of a hot-electron distribution function [K. Hess, in *Physics of Nonlinear Transport in Semiconductors*, edited by D. K. Ferry, J. R. Barker, and C. Jacoboni (Plenum, New York, 1980); S. E. Esipov and Y. B. Levinson, Adv. Phys. **36**, 331, (1987)] above the optical-phonon threshold at low densities of the electron gas (below $\sim 10^{17}$ cm^{-3}). With the reduced electron-electron collision rate, the high-energy tails of the distribution can be strongly depressed—compared to a Maxwellian curve—because of the emission of optical phonons.