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Novel Real-Space Hot-Electron Transfer Devices

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Abstract—A new class of devices based on hot-electron transfer between two conducting layers is proposed. The essential feature of these devices is a pronounced negative differential resistance (NDR) in the drain circuit, controlled by gate and substrate voltages. This allows a novel type of bistable logic element, which, although being unipolar, is comparable to the CMOS inverter in that a significant current is drawn only during switching. Another possible application is a gate-controlled microwave generator and amplifier. In the present work, the above device concepts are analyzed in the instance of GaAs/GaAlAs heterojunction realizations.

THE PURPOSE of this work is to propose a class of novel hot-electron devices based on charge injection. The principle of operation of these devices is based on heating of channel electrons by the source-to-drain electric field and a subsequent transfer of hot electrons into a subsidiary conducting layer, separated from the main channel by a specially designed built-in potential barrier. Because of the exponential dependence of the thermionic flux over the barrier on the electron temperature, one can expect an efficient charge injection into the subsidiary layer, resulting in a pronounced negative differential resistance (NDR) in the source-to-drain circuit.

In principle, the idea of using a real-space hot-electron transfer to produce an NDR effect is not new. Hess and his coworkers [1] proposed that negative resistance may arise in layered heterostructures due to hot-electron transfer from high-mobility GaAs channel layers to low-mobility GaAlAs layers. In our case the transfer occurs between two conducting electrically isolated from each other and separately contacted layers.

The blocking barrier between the two conducting layers can be organized in two distinct ways using: 1) graded (e.g., $Ga_x Al_{1-x} As$) barriers [2], or 2) planar-doped triangular

barriers [3]. In the latter case, the device can be implemented using silicon as well as III–V compound semiconductors. A blocking barrier of the camel-diode type [4] can be also produced by ion implantation. To be specific, we shall restrict our discussion to GaAs/GaAlAs heterostructures.

An important advantage of the proposed device concept is the possibility of controlling the negative resistance by applied voltages. Thus the device can be regarded as a *negative resistance field-effect transistor* (NERFET). A typical NERFET structure as well as the energy band diagram in the working section of the device is shown in Fig. 1. Top layers of the structure, including the main channel, represent a selectively doped heterojunction FET [6]. The key new element consists of a graded $Al_x Ga_{1-x} As$ barrier separating the channel from a highly conducting substrate.

Consider first the operation of this structure as an ordinary FET. For the drain voltage exceeding the gate voltage, $V_D > V_G$, the device is in a saturated-current regime due to the pinchoff effect [5]. As is well known, electrons in the pinchoff region are heated by the source-to-drain field and can be characterized by an electron temperature T_e, which may significantly exceed the lattice temperature T.

In the NERFET structure the enhanced electron temperature gives rise to a thermionic flux over the barrier into the conducting substrate. Assume first that the substrate is electrically disconnected from the source. The electron concentration in the high-field region of the channel is determined by the condition of equilibrium between the hot-electron system in the channel and "cold" electrons in the substrate. Depletion of the channel due to hot-electron emission gives rise to an induced charge density on the boundary of the conducting substrate adjacent to the barrier. This means that the electric field of the positive fixed charge, responsible for the creation of the interface channel, penetrates into the bulk thus lowering the barrier for usual thermionic emission from
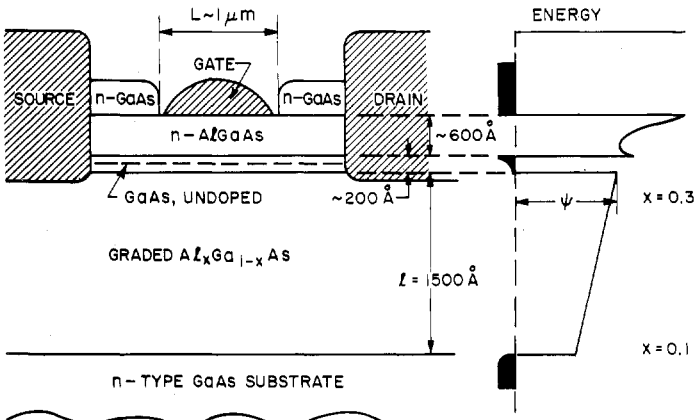
Fig. 1. NERFET structure and energy-band diagram. Regions, where the electron gas is degenerate are indicated in black on the band diagram.

the substrate into the channel. Let the initial electron charge density (without the hot-electron transfer) in the field region of the channel be σ_0. Then the hot electron density $\sigma(T_e)$ in the pinchoff region of the channel is determined by the balance of fluxes over the barrier

$$\frac{\sigma}{\Delta} \sqrt{\frac{kT_e}{2\pi m}} \ e^{-e\psi/kT_e} = AT^2 e^{-e[\psi - \frac{(\sigma_0-\sigma)l}{e}]/kT} \qquad (1)$$

where ψ and l are, respectively, the barrier height and thickness (Fig. 1), Δ is the channel thickness, e the dielectric permittivity, and m the effective mass. Analysis of (1) shows that at low heating one has $\sigma \propto T_e^{-3/2}$, whereas for high electron temperatures $\sigma \propto \exp(e\psi/kT_e)$. Transition between the two regimes occurs when $\sigma(T_e) \approx ekT/el$.

The (channel) drain current I (per unit gate width) is given by

$$I = \sigma v_s \qquad (2)$$

where v_s is the saturation velocity. Note, that in the absence of hot-electron transfer one can also write a similar relation $I_s = \sigma_0 v_s$, with I_s being the FET saturation current density.

As seen from (1) and (2), the hot-electron transfer leads to a significant lowering of the drain current. Let us make simple estimates. In the paper by Dilorenzo et al. [6], a saturation current density $I_s = 16$ mA/mm was observed at $V_D \approx 0.2$ V ($T = 77$ K). This corresponds to $\sigma_0 \equiv I_s/v_s \approx 10^{11} e/\text{cm}^2$ (although the channel concentration at $V_D = 0$ was $\approx 6 \cdot 10^{11} e/\text{cm}^2$). Assume a barrier of height $\psi = 0.4$ V and thickness $l = 1000$ Å. From (1) it follows that a strong depletion of the high-field region, $\sigma \ll \sigma_0$, occurs already at $T_e \approx 150 - 200$ K. On the other hand, according to Monte Carlo calculations for bulk GaAs [7], the electron temperature in the high-field region can be much greater, viz. $T_e \approx 800$–1000 K. At $T = 77$ K this would imply a complete depletion of the pinchoff region and an exponentially strong NDR.

The gate voltage V_G controls $\sigma_0 = I_s/v_s$ through the saturation current $I_s(V_G)$. As can be seen from the above equations, the NDR effect in the NERFET is a strong function of σ_0. The higher σ_0, the less efficient is the depletion of the pinchoff region of the channel. Physically, this is due to the fact that the barrier height for thermionic emission of "cold"
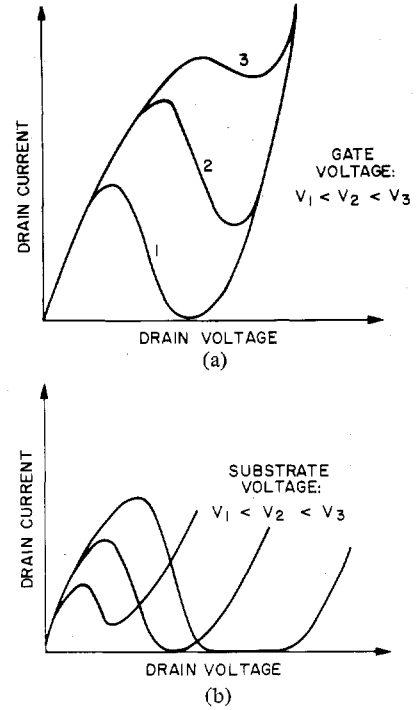

Fig. 2. Expected current–voltage characteristics in the drain circuit of a NERFET. (a) Floating substrate configuration. (b) Biased substrate configuration.

electrons from the substrate decreases linearly with the amount of charge transferred, viz. $\Delta\psi = l[\sigma_0 - \sigma(T_e)]/e$.

At higher V_D another current path also becomes important, namely the thermionic emission from the substrate directly into the drain. This current represents a thermoelectric effect induced by electron heating. Indeed, in the floating-substrate arrangement we are considering, the voltage $U = \Delta\psi$ is a thermal e.m.f., which developes due to the hot-electron transfer into the substrate. It is applied to the substrate-to-drain triangular-barrier diode in the forward direction.

Fig. 2(a) shows schematically the expected family of $I_D - V_D$ curves for different gate biases and floating substrate. It is clear that for an effective operation of the NERFET the NDR range should occur before the onset of the thermionic curent. As discussed above, higher V_G suppresses the NDR.

Next, we consider the situation when the substrate is no longer floating, but is biased positively relative to the source. In this case the heating of channel electrons does not induce charge on the substrate. Nevertheless, we can still expect a negative differential resistance in the drain circuit. Depletion of the channel will now occur owing to carriers drifting with the saturated velocity on the downhill slope of the graded barrier. This represents a space-charge limited current driven by the thermoelectric power of hot electrons. The surface density of charge $\Delta\sigma$ dynamically stored on the barrier, is proportional to the density J of the substrate current, $\Delta\sigma = Jl/v_s$. If the substrate bias is greater than the space-charge potential, $V_{SUB} > \Delta\sigma l/2e$, then the substrate current should be a weak function of V_{SUB} (implying a high differential impedance circuit). This situation is analogous to that in a vacuum diode in saturation. Increasing the electron temperature (by the drain bias) results in an enhanced injection into the substrate, just like the anode current in the vacuum diode

responds to increasing temperature of the cathode filament. If $\Delta\sigma \approx \sigma_0$, then almost all the current leaving the source will be collected in the substrate. Since the impedance in the substrate circuit is higher than that in the source-to-drain circuit, we have a voltage amplification. This is quite analogous to the bipolar transistor in its common-base configuration (with the notable exception that instead of the minority-carrier injection we are dealing here with *charge* injection of hot electrons, an entirely unipolar process). The expected family of current-voltage characteristics of the NERFET in the biased substrate configuration is shown qualitatively in Fig. 2(b). A quantitative analysis of the NERFET operation in the biased-substrate configuration should take into account the nonuniform distribution of charge σ and substrate current density J along the channel. Because of the current continuity both σ and J fall off exponentially between the pinchoff point and the drain.

The negative resistance in the drain circuit can be used for a broad-band amplification and generation of microwaves. Our estimates show that the cutoff frequency of oscillation in the NERFET drain circuit at a fixed positive substrate bias is in the millimeter-wave region. The limiting times correspond to the electron transit on the downhill slope of the graded barrier and in the high-field portion of the channel, both of order a few picoseconds. Another limitation (probably less restrictive) arises due to the finite equilibration time within the hot-electron subsystem. The time scale for this process (the energy relaxation time) is similar to that for the velocity overshoot [5, p. 339].

The negative differential resistance of the NERFET allows us to devise a novel high-speed logic element. When two NERFET's are connected in series and the total applied voltage, *VDD* is greater than twice the critical voltage for the onset of NDR in a single device, then an instability occurs. One of the devices will necessarily be in a low-field mode, while the other will take practically the entire voltage. This is a general feature of any circuit containing two identical n-type NDR elements in series. By applying a gate voltage, we can control which of the two devices will contain the high-field domain. Consider the circuit, shown in Fig. 3(a) and (b). Both devices are assumed to be identical. The substrate is either floating or connected to a positive end of the battery through a large resistance. When the gate of the bottom transistor is biased positively, then the high-field domain is located in the top transistor and vice versa. As we switch the gate voltage, the induced charge (indicated by vertical dashes in Fig. 3) moves in the substrate from one gate to the other. Once established (by a pulse of the gate voltage) the high-field domain will stay in the same device indefinitely, until the situation is reversed by another pulse of opposite polarity.

To summarize, we have proposed a new structure, called the NERFET, which employs hot-electron transfer between two conducting layers separated by a barrier. We discussed the expected characteristics of this structure in its two principal configurations corresponding to floating or biased substrate. The first NERFET structures have, in fact, been fabricated recently [8], with encouraging results. We observed a well-pronounced negative resistance, strongly influenced by the gate and substrate voltages. At 77 K, the negative
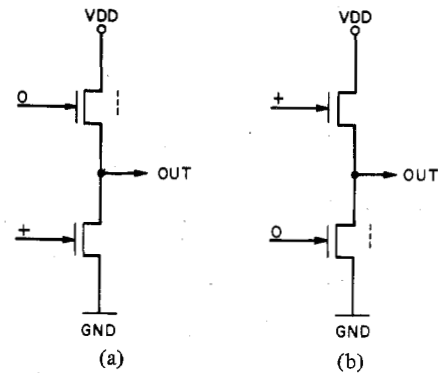

Fig. 3. NERFET logic. Substrate is either floating or biased through a large resistance. (a) High-field domain is in the top transistor; $V_{out} = G_{ND}$. (b) Domain is in the bottom transistor; $V_{out} = V_{DD}$. Vertical dashes indicate position of the induced charge.

differential resistance appears both in the floating- and biased-configurations, with the peak-to-valley ratios of more than 30 (the peak current being about 100 mA for a 1-μm $\times$ 250-μm gate). Even at room temperature, a strong NDR (ratio of about 7) is seen when the substrate is positively biased.

Even though the microwave performance of the NERFET remains to be tested experimentally, we have grounds to believe that our device may become useful as an efficient generator of microwaves in the millimiter range, controllable and tunable by the gate and substrate voltages. The NERFET in its biased-substrate configuration exhibits no unwelcome memory effects. Ideally, its frequency of oscillation should be limited only the energy relaxation time and the times of flight of electrons over the regions of high electric field.

We have also discussed a novel bistable logic element formed by two NERFET's in series. The principal advantage of this element which stems from the deep negative differential resistance in the NERFET's drain circuit, lies in its low power dissipation in both logic states. In order to use this advantage, it is essential to employ the device in its floating-substrate configuration, since otherwise power would be dissipated by the substrate current. High-speed low-power logic applications of the NERFET appear to us very promising.

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