Automatic generation of equivalent circuits from device simulation

A. Pacelli*†, M. Mastrapasqua*, M. A. Alam*, and S. Luryi†

* Bell Laboratories, Lucent Technologies
600 Mountain Avenue, Murray Hill, NJ 07974, pacelli@lucent.com
† State University of New York, Stony Brook, NY 11794-2350, Serge.Luryi@sunysb.edu

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ABSTRACT

We present a novel methodology for the direct extraction of equivalent circuit models from device simulation. The circuit topology is physically based, i.e., each voltage node corresponds to a quasi-Fermi level or to an electrostatic potential. Circuit equations and branch-constitutive equations are derived from the Poisson and continuity equations. Although only d.c. simulation results are employed, the model achieves a.c. predictive power by including charge-storage elements as capacitors. The technique has been implemented for one-dimensional devices. Examples are shown for *pn* junctions including high frequency and high injection regimes. An example of optical response of a phototransistor is presented, demonstrating the applicability of the method to optoelectronic and three-terminal devices.

Keywords: Compact models, equivalent circuits, RF circuit simulation, semiconductor device simulation

1 INTRODUCTION

A compact device model for circuit applications should be reliable and physically based. Currently, model generation is performed either by fitting physical analytical expressions to experimental data [1], or by table-based approaches [2], [3]. In the former case, the procedure is laborious and time-consuming. Moreover, the physical meaning of the circuit elements is often lost when the model is stretched beyond its original range of application. In the table-based approach, the model parameters usually have no clear physical interpretation.

In this work we present a general methodology to derive equivalent-circuit topologies and elements, starting from physical device simulations [4]. The basic circuit building block is similar to that originally devised by Sah in the limit of a small semiconductor region and for linear charge transport [5]. We have modified and extended the basic building block model by allowing for regions of finite size. A more general expression has also been introduced for the electron and hole currents, allowing the inclusion of effects such as velocity saturation and MOS surface mobility. The technique has been implemented in a one-dimensional model extraction code.

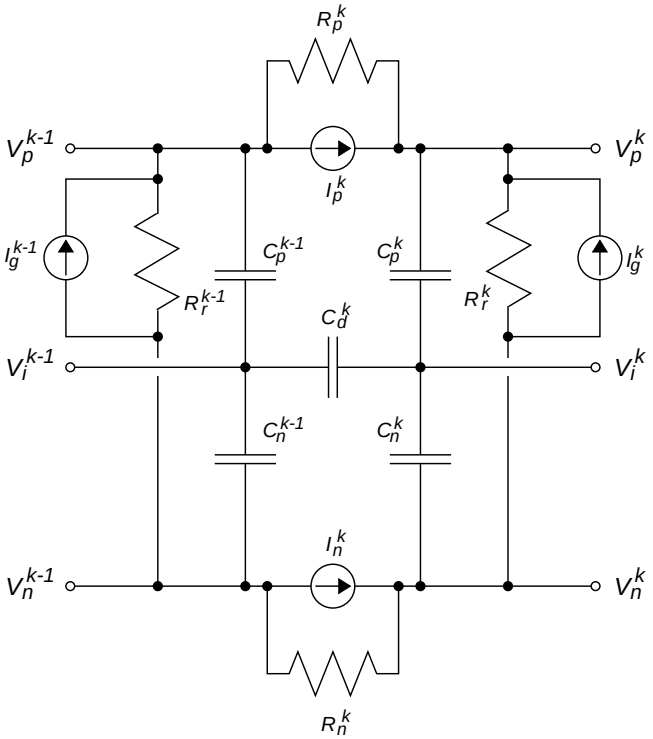

Figure 1: Equivalent circuit representation of the Poisson and continuity equations.

2 DERIVATION OF CIRCUIT EQUATIONS

As originally shown by Sah [5], for a vanishing semiconductor volume a circuit representation can be directly derived for the Poisson and continuity equations. By using the box-integration technique [6], we have rigorously extended this approach to a semiconductor region of finite size. The resulting small-signal equivalent circuit is shown in Fig. 1 for a one-dimensional slab of semiconductor, bounded by coordinates x_{k-1} and x_k. Voltages V_p^k, V_n^k, and V_i^k are respectively the values of the electron and hole quasi-Fermi level and the electrostatic potential at x_k. C_p^k and C_n^k are the hole and electron charge-storage capacitance elements at node k, while C_d^k is the dielectric capacitance connecting nodes $k-1$ and k. The current generator I_p^k is controlled by the four voltages $(V_p^{k-1}, V_p^k, V_i^{k-1}, V_i^k)$, and together with

the resistor R_p^k supplies a general model for hole transport (analogously for electron transport). The resistor R_r^k and the current generator I_g^k model recombination and generation, respectively.

Numerical values of all the elements are computed from d.c. device simulation. For example, the charge storage capacitances are defined as

$$C_p^k = \frac{\delta Q_p^k}{\delta(V_p^k - V_i^k)} \quad (1)$$

$$C_n^k = \frac{\delta Q_n^k}{\delta(V_i^k - V_n^k)} \quad (2)$$

where δ denotes the small-signal d.c. response as obtained by numerical simulation. Q_p^k and Q_n^k are the absolute hole and electron charges obtained from the numerical solution by integrating over a finite volume of semiconductor. The current generator I_p^k is defined as

$$I_p^k = G_{mp}^k(v_i^{k-1} - v_i^k) + G_{fp}^k(v_p^{k-1} - v_i^{k-1}) + G_{rp}^k(v_p^k - v_i^k). \quad (3)$$

The three conductances G_{mp}^k, G_{fp}^k, and G_{rp}^k, and the resistance R_p^k (and G_{mn}^k, G_{fn}^k, G_{rn}^k, R_n^k for electrons) are also computed from the device simulation. A minimum constraint is that the resulting circuit must replicate the d.c. behavior of the device, i.e., the correct conductance at low frequency. This condition is met by requiring that the generator I_p^k supplies a current equal to the d.c. value from the device simulator, when the same voltage boundary conditions are applied. One such equation must be satisfied for each generator. The a.c. behavior is matched by introducing further constraints. For example, the majority hole behavior in a quasi-neutral p-region is well described by the resistor R_p^k. On the other hand, the transconductances G_{fp}^k and G_{rp}^k are more appropriate for modeling the diffusion of minority holes. The transconductance G_{mp}^k represents the dependence of current on the electrostatic potential drop, i.e., the average electric field, and is useful to describe field-dependent mobility variations. In one dimension, the velocity saturation effect can be described by this quantity. In two dimensions, the effect of a transverse electric field may also be modeled, such as MOSFET surface mobility. These physical criteria are converted into additional equations used to assign numerical values to all circuit elements.

A small-signal model extraction code has been implemented for one-dimensional devices. Drift-diffusion solutions were obtained from the device simulator PADRE [7], however no special features of this simulator were used. Therefore, any commercial simulation code may be employed. The different areas of the device (quasi-neutral regions, depletion regions) are first automatically identified from the electric field profile. Each of the

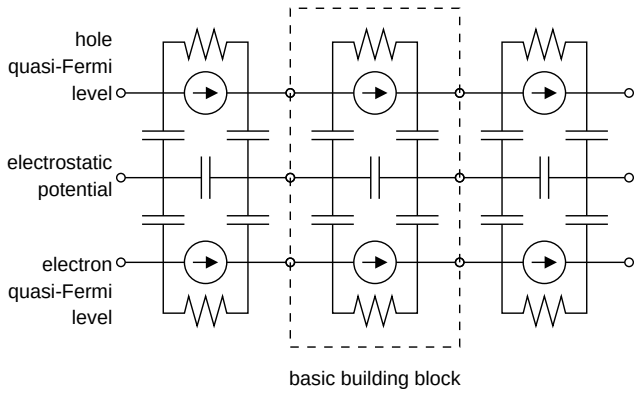

Figure 2: Equivalent circuit topology. Each of the building blocks corresponds to a semiconductor region. The current generators are frequency-independent and controlled by the terminal voltages of the five capacitors in each block. For clarity, the circuit elements modeling generation-recombination have been omitted.

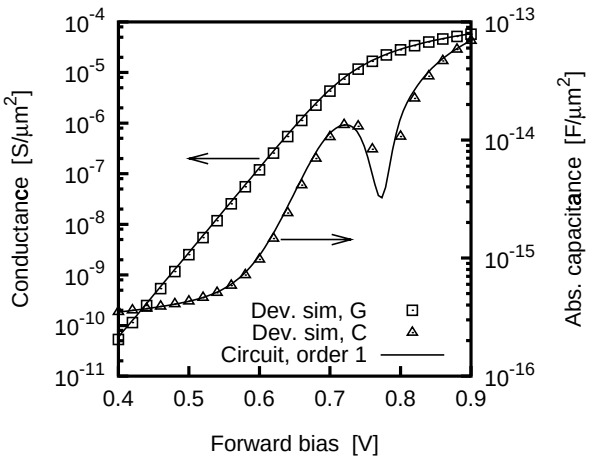

Figure 3: Small-signal conductance and capacitance at 100kHz for a symmetric pn junction with 5μm long p and n regions of doping 10^{16}cm^{-3}. Symbols show device-simulation results. The first-order circuit (solid line) had three circuit blocks, one for each quasi-neutral base, and one for the depletion region (Figure 5). The dip in the capacitance corresponds to a change of sign at 0.77 V.

regions can optionally be partitioned into sub-regions for higher accuracy. The model parameters are then computed for each region from device simulation. The complete circuit is finally obtained by joining the circuit blocks as shown in Fig. 2. After model generation, the circuit may be simplified by circuit transformation, e.g., by lumping capacitors connected in parallel.

3 APPLICATIONS

As a first example, we consider a prototype pn junction as described in Ref. [8]. Each of the n and p regions is 5 μm long, with constant doping. The car-

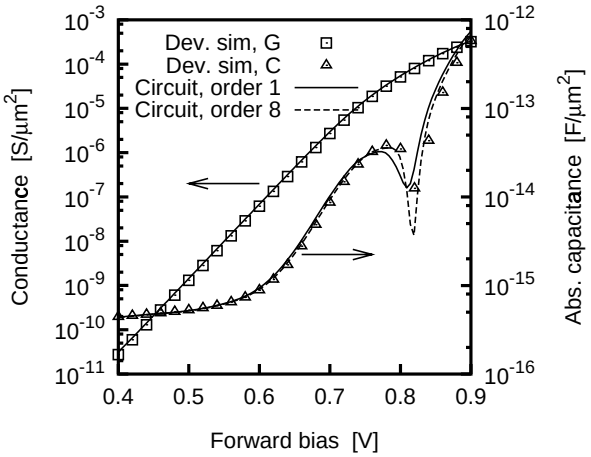

Figure 4: Small-signal conductance and capacitance at 100kHz for an asymmetric *pn* junction (doping $10^{18}/10^{16}\mathrm{cm}^{-3}$). Results from the first order circuit (three circuit blocks) and the 8th-order (17 blocks total, 8 for each of the quasi-neutral regions, and one for the depletion region) are shown. The dip in the capacitance corresponds to a change of sign at 0.82 V.

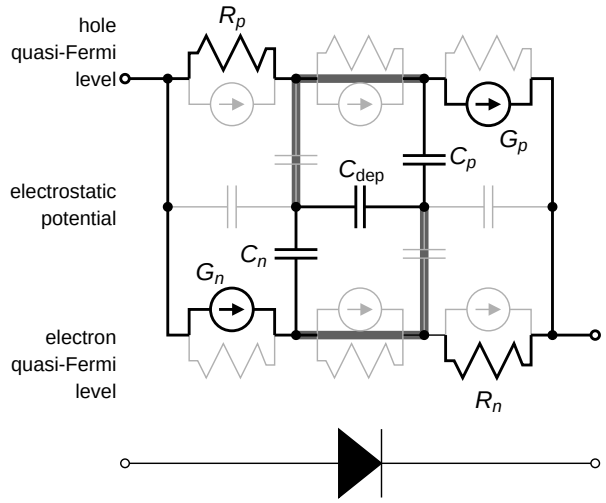

Figure 5: First-order (three-block) equivalent circuit of a *pn* junction. The elements drawn in black are those which implement the minimum device functionality. The elements drawn in grey are only required for accurate high-injection and high-frequency modeling. The heavy dark lines highlight elements which reduce to short circuits in the low-injection, low-frequency case.

rier mobility is assumed doping- and field-independent, and equal to $1000\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ for both electrons and holes. Figures 3 and 4 show the low-frequency conductance and capacitance as functions of forward bias, as computed for two *pn* junctions. The first junction is symmetrical, with a doping of $10^{16}\mathrm{cm}^{-3}$ on both sides (Fig. 3), while the other is approximately one-sided ($10^{18}/10^{16}\mathrm{cm}^{-3}$, Fig. 4). The plots of Figs. 3 and 4 were obtained by computing a different small-signal circuit for each bias point, while keeping the circuit topology unchanged. The extraction is accurate even in the high injection region, where inductive behavior occurs [8], [9]. The first-order equivalent circuit shown in Fig. 5 comprises one circuit block for each of the quasi-neutral regions, and one additional block for the depletion region. The resistors model the quasi-Fermi level drops due to ohmic transport in the majority regions, while the controlled generators correspond to minority-carrier diffusion. Note that, following Sah, the electrostatic potential is explicitly introduced as a model variable. This feature overcomes the limitations of simpler models, as discussed in Ref. [8]. While this basic topology is adequate for low-frequency modeling, an increase in complexity may be necessary to account for transmission-line properties of the quasi-neutral regions at high frequency. Figure 6 shows the good accuracy of the model frequency response well above the diode cutoff frequency, especially for the higher-order models, where multiple circuit blocks are employed for the quasi-neutral regions.

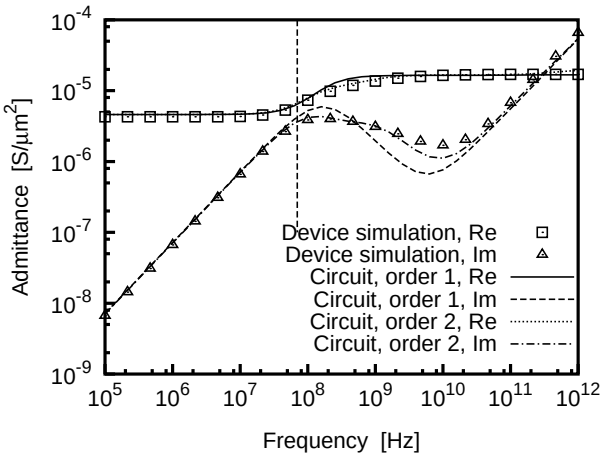

Figure 6: Frequency response (real and imaginary part of the small-signal admittance) for the first- and second-order model of Fig. 3, at a forward bias of 0.7V. The dashed line indicates the diode cutoff frequency.

In order to investigate the adequacy of the model for three-terminal applications, we have simulated an *npn* phototransistor. The device doping and principle of operation is illustrated in Fig. 7. The light-collection region is about $1\,\mu$m wide, and is almost fully depleted at a collector-to-emitter voltage of 10 V. The base terminal is left open. When the device is uniformly illuminated, electron-hole pairs are generated throughout the material. The current I_1 due to holes generated in the base-collector depletion region is injected into the base, and multiplied by the transistor current gain β (Fig. 7, inset). The amplified current $I_2 = \beta I_1$ reaches the collector after a delay due to the charging of the base-emitter junction. In the circuit model, photogeneration is modeled by a current source for each building

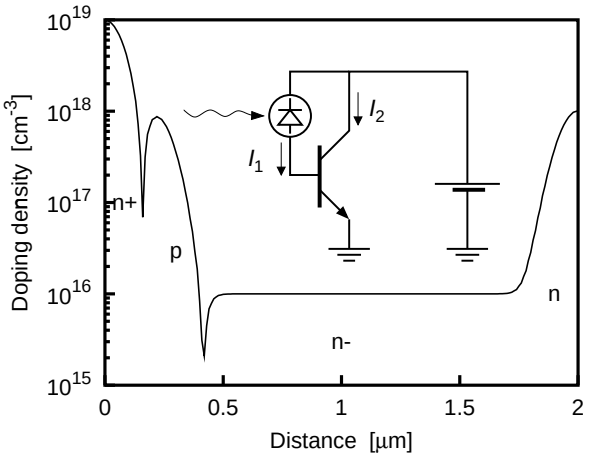

Figure 7: Doping profile of *npn* phototransistor. The uniformly-doped collection region is about 1μm wide. The inset shows the schematics of device operation. The collector bias voltage is 10 V.

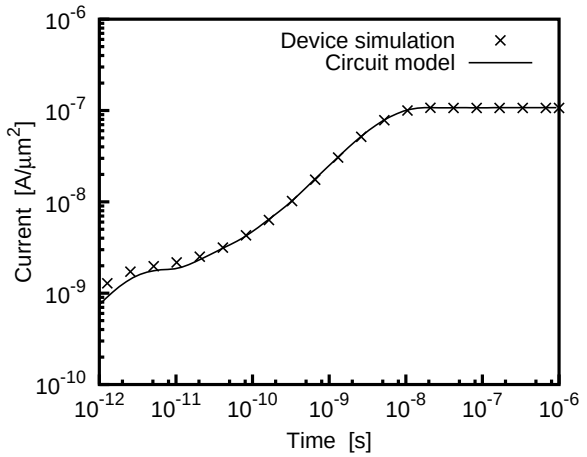

Figure 8: Time transient of output current for the phototransistor of Fig. 5, for a step increase of light intensity. The initial small increase of current is due to the arrival of primary photocurrent I_1 to the collector, while the second step is due to the current $I_2 = \beta I_1$ by transistor action.

block (Fig. 1). The time response of the output current to a step increase in optical intensity is shown in Fig. 8. The circuit model tracks the device simulation quite well, including the phototransistor time constant of about 10 ns. We remark that all the circuit models were automatically obtained, without any manual calibration of the parameters.

4 CONCLUSIONS

We have presented a new approach to equivalent circuit derivation, which requires only d.c. device simulations to generate a full small-signal a.c. device model. The method has been shown to correctly model the high-injection and high-frequency behavior of *pn* junctions, and also to naturally include optical effects. Although the technique has so far been implemented for one-dimensional devices, the circuit topology easily scales to higher dimensionality, and an extension to 2D simulation is in progress.

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