# Dependence of the off-state current in polycrystalline silicon thin film on electric field in the channel

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We correlated the *off-state* current in polycrystalline silicon (polysilicon) thin film transistor (TFT) with the peak electric field in the channel of the device. We investigated $p$-channel TFTs with different gate oxide thicknesses, at varying gate and drain biases. The electric fields in the channel of the devices under these experimental conditions were calculated using both process and device simulators, and the experimental *off-state* current was plotted against simulated fields. We found that in a wide range of electric fields the current exhibits a nearly exponential behavior. Different combinations of the drain and gate biases produce nearly the same *off-state* current, provided the calculated peak field is the same; moreover, curves corresponding to different gate oxide thicknesses overlay each other. Our results are compatible with the model of the *off-state* current as being due to the field emission at grain boundaries.

The presence of grain boundaries has a profound effect on the performance of polycrystalline silicon (polysilicon) thin film transistor (TFT). In the *off-state* of the device, they are responsible for generation of the *off-state* current. This current is believed to be caused by the field emission via in-gap states associated with the grain boundaries.[1] In this work we correlated experimentally measured field-emission current in $p$-channel TFTs with the channel field numerically simulated at the experimental conditions. The variation in the electric field at the drain of the device was achieved by varying the gate and drain voltages as well as the thickness of the gate oxide.

We investigated devices with an inverted structure, with the gate underneath the channel (Fig. 1). Polysilicon of the inverted gate was heavily doped with phosphorus. The gate oxide was formed by low pressure chemical vapor deposition (LPCVD). As-deposited, the oxide was 250 Å thick; variations in $d_{ox}$ were obtained by submerging groups of wafers in a 100:1 HF solution for different lengths of time. The actual thickness of the gate oxide was determined by ellipsometry. Device channel was formed by the CVD of a 400 Å amorphous silicon layer with a subsequent grain-size enhancing solid phase growth anneal,[2] resulting in an average grain size of 2500 Å. Source and drain regions were formed by patterning and $BF_2$ implantation. For our measurements, we chose devices with as-drawn gate length of 1.2 $\mu$m; we estimate the outdiffusion from the source and drain regions into the channel at the processing heat cycle (the highest temperature 800 °C) to be 0.1 $\mu$m, therefore, the actual channel length was 1.0 $\mu$m.

To find the dependence of the *off-state* current on the electric field in the channel, *off-state* current-voltage ($I$-$V$) characteristics of each TFT were measured as a function of the drain bias, for two gate biases, 0 and 1 V. Figure 2 shows the dependence of the *off-state* current on the drain bias for three gate oxide thicknesses, 130, 200, and 250 Å. Then the structure of the device with the corresponding gate oxide thickness was extracted using the process simulator PROFET[3] and fed into the device simulator PADRE[4] to obtain, for each $(V_D, V_G)$ configuration, the electric field distribution in the device. The fields were calculated as a module of a vector sum of the fields parallel and normal to the channel, $|E_{par}+E_{norm}|$. A typical *off-state* field profile along the channel at the interface with the gate oxide is shown in Fig. 3. Note a sharp peak at the drain junction of the device where the drain bias is applied. For each oxide thickness, the measured current corresponding to a certain $(V_D, V_G)$ was

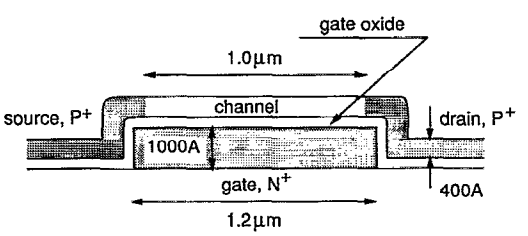


FIG. 1. Structure and dimensions of the inverted device.

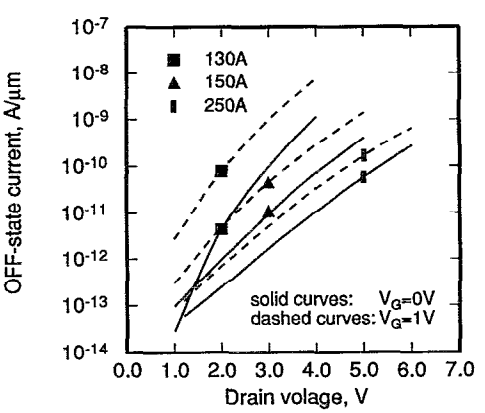


FIG. 2. Dependence of the *off-state* current on the drain voltage, at $V_G$=0 and 1 V, for different thicknesses of the gate oxide.

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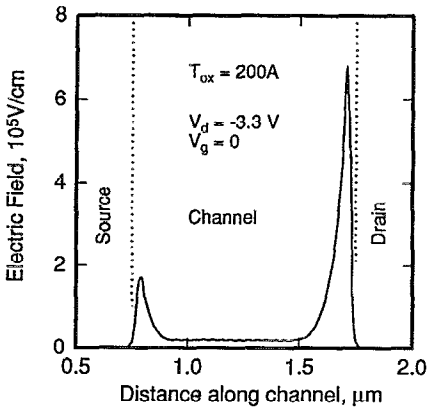


FIG. 3. Distribution of the electric field along the channel of the device at the interface with the gate oxide, for $d_{ox}$ 200 Å, at $V_D=-3.3$ V and $V_G=0$.

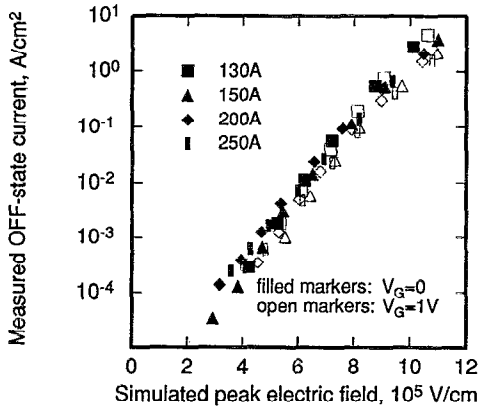


FIG. 4. The measured *off-state* current density (per unit area of the channel cross section) plotted against the calculated peak value of the electric field in the channel.

correlated with the electric field calculated at the same bias configuration.

Figure 4 shows the measured *off-state* current density, plotted against the calculated peak field value (note that the current is given in units of current per unit area of the device; this is because the *off-state* current is generated in the bulk of polysilicon rather than in the induced channel). In the range between 0.2 and 1.3 MV/cm the *off-state* current exhibits a nearly exponential behavior over six orders of magnitude. Note that different $(V_D, V_G)$ configurations produce nearly the same *off-state* current, provided the calculated peak field is the same. Moreover, curves corresponding to different gate oxide thicknesses overlay each other. This common behavior suggests a "universal" dependence of the *off-state* current on the electric field, which is compatible with the model[1] of field emission at polysilicon grain boundaries and permits its quantitative characterization.

[1] J. G. Fossum, A. Ortiz-Conde, H. Shichijo, and S. K. Banerjee, IEEE Trans. Electron Devices **ED-32**, 1878 (1985).
[2] R. B. Iverson and R. Reif, J. Appl. Phys. **62**, 1677 (1987).
[3] C. S. Rafferty, J. L. Lentz, and H. H. Vuong, *PROPHET Process Simulator User's Guide* (AT&T Bell Laboratories, Murray Hill, NJ, 1991).
[4] M. R. Pinto, 1991 ULSI Science and Technology, Electrochem. Soc. Proc. **91-11**, pp. 43-51 (1991).
[5] K. Tanaka, Harai, and S. Kohda, IEEE Electron Device Lett. **EDL-9**, 23 (1988).