Active-Gate Thin-Film Transistor

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***Abstract*—We propose a new thin-film transistor (TFT) with a lightly-doped offset built in the polysilicon gate. The offset region of the gate acts as a dielectric in the OFF state and as a conductor in the ON state. The unwelcome peak of the electric field near the drain in the OFF state is significantly reduced, as has been confirmed by two-dimensional device simulation. The key advantage of this device over conventional "passive" offset structures is that the ON current is not reduced, while the OFF current is suppressed by several orders of magnitude.**

THIN-FILM transistors (TFT's) are used in static random access memory (SRAM) technology as pull-up devices in six-transistor complementary MOS cells. In order to reduce the SRAM circuit standby power, it is important to lower the OFF state current of the TFT, which is believed to be caused by field emission at polysilicon grain boundaries in the high-field region near the drain [1]. The OFF current is significantly reduced in TFT structures with a drain offset [2] (ungated part of the channel, cf. Fig. 1(a)), which lowers the peak field in the channel. However, the added series resistance of the ungated channel portion considerably reduces the ON state current, thus degrading the cell stability. It is desirable to have a device which would have the properties of a drain offset structure in the OFF state, while behaving like a fully gated device in the ON state. This is accomplished in a new thin-film device, the active-gate thin-film transistor (AG TFT), proposed in the present work.

The key feature of the new structure, shown in Fig. 1(b), is the undoped or lightly doped part of the gate which overlays the channel region near the drain; the gate is heavily doped only in the region adjacent to the source. When the device is in the ON state, the lightly doped region is in accumulation and provides the field effect for the channel conductivity. In the OFF state, the lightly doped region is depleted and acts like a drain offset. The main advantage of the AG TFT lies in the fact that the offset built in the gate does not decrease the drain ON current. In the present work, we study the feasibility of the AG TFT by two-dimensional device modeling. We use the AT & T simulator PADRE [3].

We consider an upright p-channel TFT with parameters typical for SRAM applications: silicon channel thickness = 400 Å, gate oxide thickness = 200 Å, gate length = 1 μm, channel length = 0.9 μm, and gate thickness = 1000 Å. The SRAM power supply is assumed to be the industry-compatible 3.3 V. The channel-layer polysilicon is normally subjected to a grain-enhanced processing (such as the solid phase growth [4]). In our model, the gate polysilicon is also assumed to have an improved grain structure. The large-grain polysilicon materials of the channel and the gate are modeled as single-crystal silicon layers with low carrier mobilities: 10 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for holes in the channel and 50 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for electrons in the gate. Since the TFT processing temperatures are usually limited to below 850°C, the device junction depths (source/channel, channel/drain, and the n^+-n^- junction in the gate) are estimated to be ~ 500 Å, mainly determined by the lateral straggle of ion implantation. The mobile carrier concentration in polysilicon may differ from the total dopant concentration due to carrier trapping by grain boundaries. The active dopant concentration is taken as a modeling parameter.

Fig. 2 shows the simulated OFF state electric field distribution in the channel along the gate oxide interface. The high peak of 0.7 MV/cm near the drain corresponds to the conventional case, when the gate is doped uniformly and heavily (10^{20} cm^{-3}). The second curve corresponds to the case when the 0.5-μm portion of the gate, adjacent to the drain (which we shall refer to as the gate offset), is doped to only 10^{15} cm^{-3}; the peak field is reduced to 0.3 MV/cm, which is nearly the same level as for a conventional 0.5-μm drain offset. Keeping the same geometry and considering the peak field value as a function of the dopant concentration in the gate-offset region, we found that the field increases rapidly between 10^{16} and 10^{18} cm^{-3}, while at concentrations below and above this range the peak field is approximately constant. Considering the dependence of peak field on the gate offset length, we found that the field is strongly reduced already at small offsets, mostly in the range between 0 and 0.3 μm; extension above 0.5 μm brings no further reduction.

The electron concentration in the polysilicon gate along the interface with the gate oxide is plotted in Fig. 3 both for the OFF state ($V_G = 0$, $V_D = -3.3$ V) and the ON state ($V_G = V_D = -3.3$ V). In the OFF state, the concentration drops abruptly at the n^+-n^- junction, indicating that the offset region of the gate is completely depleted. In the ON state, the electron concentration in the gate offset never drops below 10^{18} cm^{-3}. The total sheet electron concentration in the gate offset area ($\approx 2 \times 10^{12}$ cm^{-2}) is quite sufficient to induce an adequate channel conductivity. The calculated ON state drain current is practically unaffected by either the length of the gate offset or its doping.

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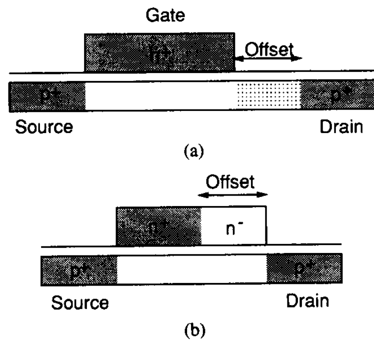

Fig. 1. Schematic cross section of a p-channel polysilicon thin-film transistor. (a) Conventional drain-offset structure. (b) Active-gate TFT with an offset built in the gate layer.

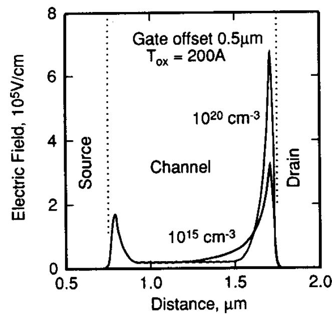

Fig. 2. Calculated electric field profile in the channel for two doping levels in the gate offset region. The device is in its OFF state with $V_G = 0$ V and $V_D = -3.3$ V.

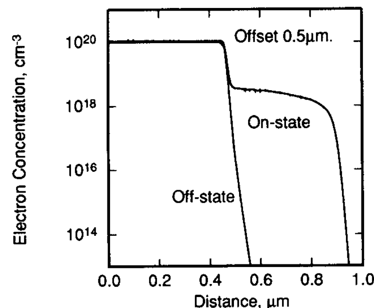

Fig. 3. Calculated electron concentration in the active gate along the oxide interface in both the ON state (V_G and $V_D = -3.3$ V) and the OFF state ($V_G = 0$ and $V_D = -3.3$ V).

To find the dependence of the OFF state current on the electric field in the channel, we have measured the characteristics of a conventional TFT (no offset) as a function of both the gate and the drain biases. For each $\{V_D, V_G\}$ configuration, the corresponding distribution of the electric field along the channel of the device is then simulated by PADRE. Fig. 4 shows the measured OFF state current density, plotted against the calculated peak field value. In the range between 0.2 and 1.3 MV/cm, the OFF state current exhibits a nearly exponential behavior over six orders of magnitude. Most importantly, different $\{V_D, V_G\}$ configurations produce nearly the same OFF state current, provided the calculated peak field is the same. Moreover, curves corresponding to different gate oxide thicknesses overlay each other. This common behavior suggests a "universal" dependence of the OFF state current on the electric field, which is compatible with the model [1] of field emission at polysilicon grain boundaries and permits its quantitative characterization. For devices similar to those modeled in Fig. 2, the universal dependence gives an estimate of the expected reduction in the TFT OFF state current by more than two orders of magnitude. For thinner oxides this improvement is still larger. The calculated reduction is identical to that obtained in TFT's with a conventional drain offset of comparable length.

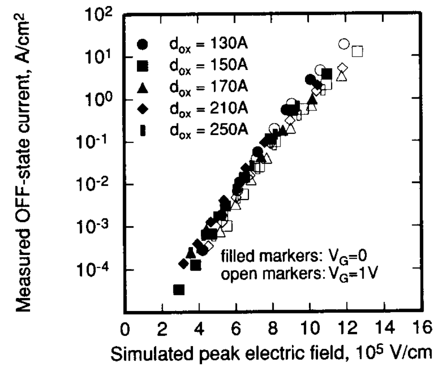

Fig. 4. The measured OFF state current density (per unit area of the channel cross section) plotted against the calculated peak value of the total electric field in the channel, obtained in PADRE simulations corresponding to the experimental bias configuration.

To summarize, we have proposed and simulated a new type of TFT with a lightly doped offset built in the polysilicon gate. The offset acts as a field-reducing dielectric in the OFF state and as a conducting part of gate in the ON state. The field-effect activity inside the gate is essential for the device performance. The significant advantage of this device over conventional "passive" offset structures is that the ON current is not reduced. The processing of the active gate TFT does not seem to be any more demanding: the device performance is sensitive neither to the mask alignment for the partial gate implant nor to the exact level of the doping (below 10^{16} cm^{-3}) in the gate offset. While the most obvious application of AG TFT is for p-channel pull-up device in SRAM circuits, its outstanding features can be used in large-area electronics applications as well.

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