Multiterminal Light-Emitting Logic Device Electrically Reprogrammable Between OR and NAND Functions

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Abstract—**A monolithic multiterminal logic device that functions both optically and electrically as an "ORNAND" gate, is demonstrated for the first time. The device, based on the real-space transfer of hot electrons into a complementary collector layer, has been implemented in an InGaAs/InAlAs/InGaAs heterostructure grown by molecular beam epitaxy. Excellent performance is obtained at room temperature. The collector current and the optical output power both exhibit the *or* and the *nand* functions of any two of the three input terminals, these functions being interchangeable by the voltage on the third terminal.**

I. Introduction

An important direction in microelectronics research is the development of new *functional devices*, which can perform logic tasks that would normally require an assembly of several transistors. The charge injection transistor (CHINT) [1] offers interesting opportunities in this context. The CHINT concept refers to a class of devices based on the real-space transfer (RST) [2], [3] of hot electrons between independently contacted conducting layers. Several functional devices employing this principle have been discussed in the literature [4]–[11].

A generic CHINT structure is illustrated in Fig. 1. One of the conducting layers, the emitter, plays the role of a hot-electron cathode, with the heating voltage applied to the contacts S and D. The other conducting layer, the collector, is separated by a heterostructure barrier. The RST effect manifests itself in the increase of the collector current I_C at a constant positive collector bias V_C, when a sufficiently high heating bias V_{DS} is applied. Recently, we have demonstrated [10], [11] an optoelectronic version of CHINT in which the RST occurs in a collector layer of *complementary* conductivity type and results in a luminescence signal whose power P_L is to a large degree proportional to I_C.

A fundamental property of RST transistors, essential in our present discussion, is the *symmetry equivalence* [12],

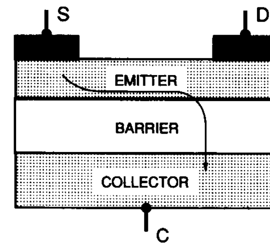

Fig. 1. Schematic diagram of a charge injection transistor. Emitter electrons heated up by the field applied between electrodes S and D undergo real-space transfer, as indicated by the arrow. By symmetry, the output current I_C at a fixed collector bias V_C is an exclusive-OR function of the input voltages: I_C = **xor**(V_S, V_D).

[13] between the internal states $S[V_D, V_C]$ of the device at different external bias configurations

$$S[V_D, V_C] \rightleftarrows S[-V_D, (V_C - V_D)]. \tag{1}$$

This correspondence follows from the reflection symmetry in the plane normal to the source–drain direction which cuts the channel in the middle. Although a similar relation exists between internal states $S[V_D, V_G]$ in a field-effect transistor, there is an important difference in that the CHINT collector is the output terminal and the symmetry expressed by (1) implies that the output current is invariant under an interchange of the input voltages V_S and V_D. Thus the device exhibits an exclusive-OR (**xor**) dependence of the collector current (and output light in a complementary device) on the input voltages, regarded as binary logic signals. The optoelectronic **xor** operation of a complementary CHINT has been demonstrated experimentally [10], [11].

Even more powerful logic functionality is obtained in an RST device with three input terminals [6]. This device, which we shall refer to as the ORNAND gate, has a cyclic three-fold symmetry, Fig. 2. Its truth table corresponds to **ornand**$(\{V_j\}) \equiv$ **norand**, where

$$\mathbf{norand}(\{V_j\}) = (V_1 \cap V_2 \cap V_3) \cup (\overline{V}_1 \cap \overline{V}_2 \cap \overline{V}_3) \tag{2}$$

and the symbols $\cap$, $\cup$, and $\overline{A}$ stand for logic functions **and**, **or**, and **not***A*, respectively. The **ornand** equals

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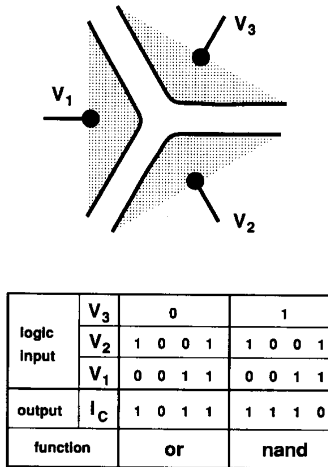


logic input	V_3	0				1			
	V_2	1	0	0	1	1	0	0	1
	V_1	0	0	1	1	0	0	1	1
output	I_C	1	0	1	1	1	1	1	0
function		or				nand			

Fig. 2. Principle of the multiterminal logic device ORNAND. Three input terminals arranged with a three-fold cyclic symmetry (top figure) define three channels 1–2, 2–3, and 3–1. The RST current I_C as a function of the voltages V_1, V_2, and V_3, regarded as logic signals, obeys the truth table shown. The value of I_C is low (logic-0) in two states when $V_1 = V_2 = V_3$ and is high (logic-1) in the other six states. By the symmetry, all the logic-1 states give the same I_C.

or(V_1, V_2) when V_3 is low, and **nand**(V_1, V_2) when V_3 is high. The electric ORNAND operation has been demonstrated [6] using an assembly of three discrete unipolar CHINT devices.

The present work reports the first realization of a monolithic ORNAND gate. The use of a complementary collector structure enables both electrical and optical output signals.

II. Epitaxial Structure and Device Fabrication

The lattice-matched InGaAs/InAlAs heterostructure has been grown by molecular beam epitaxy on a p-type InP substrate and processed by wet etching. A schematic cross section of the device is illustrated in Fig. 3. The design is based on the epitaxial contact scheme [14], in which the channel length is defined by a trench etched in the n^+ cap layer *a* while the remaining portions of the cap layer make ohmic contacts to the emitter. The 25-Å InAlAs layer *b* is used as an etch stop in the selective etching of the cap layer [15]. All patterns, including the trenches, were defined by standard optical contact lithography. The trench length is $L_{CH} = 1$ μm and the channel width is $W = 40$ μm. Instead of a triangular arrangment of the electrodes, as in Fig. 2, the required cyclic symmetry is obtained with four electrodes 1, 2, 3, $\tilde{3}$, the latter two being logically identical $V_{\tilde{3}} \equiv V_3$) though physically split.

The epitaxial structure shown in Fig. 3 is generally similar to those used in our previous studies [10], [11] of the complementary CHINT, but there are several noteworthy differences. The present structure is grown on a p-type substrate and uses a more heavily doped collector contact layer to reduce the parasitic series resistance in the collector circuit. The emitter channel is also more heavily doped to avoid its complete depletion by the surface potential and ensure a "normally-on" channel, which conducts even in the absence of a positive V_C.

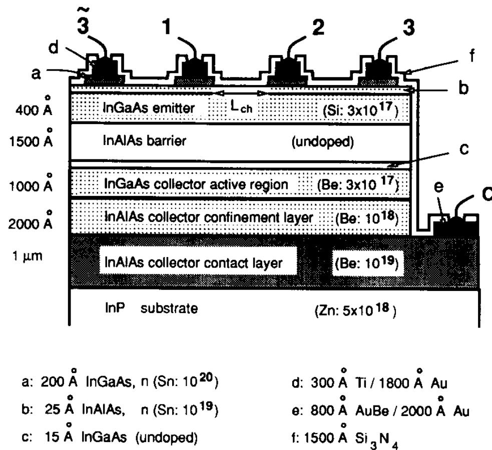


Fig. 3. Cross section of the device structure. Cyclic symmetry of an ORNAND gate results from the periodic boundary condition obtained by tying together electrodes 3 and $\tilde{3}$.

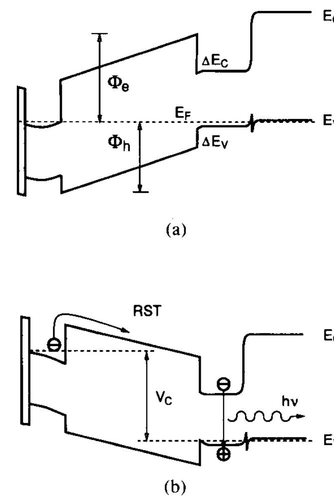


Fig. 4. Schematic energy band diagram in a device cross section under the channel in equilibrium (a) and under a positive collector bias (b).

Fig. 4(a) shows the energy band diagram of an equilibrium device. In the operating regime, corresponding to a positive collector bias, Fig. 4(b), the collector–emitter p-n junction is forward-biased and the only obstacle to current is due to the band discontinuities ΔE_C and ΔE_V of which $\Delta E_V \approx 0.2$ eV is the smaller one in the InGaAs/InAlAs system. The heterostructure barriers are sufficiently high that the collector leakage current I_C^{LKG} is relatively small even at room temperature. When the emitter electrons are heated by the lateral channel field, the electron temperature T_e substantially exceeds the lattice temperature T and a large RST injection current I_C^{RST} results. In our complementary structure, I_C^{RST} is accompanied by a 1.6-μm lu-

minescence signal, arising from the recombination of the injected electrons with holes in the InGaAs collector active region. The purpose of the p-type InAlAs layer in the collector is to spatially confine the minority carriers. The confinement is necessary for a good radiative efficiency, otherwise most of the injected electrons would reach the collector contact prior to recombination.

III. Electrical and Optical Properties of a Single Channel

The multiterminal logic device actually forms three channels: 1–2, 2–3, and $\tilde{3}$–1. Fig. 5 shows the typical room-temperature characteristics, measured in the channel $\tilde{3} \rightarrow 1$. Here and below we shall use an arrow to indicate the source → drain direction in a particular measurement. Characteristics of different channels coincide quite closely, but there is a slight asymmetry under the source–drain interchange in a single channel, due to an unavoidable off-center misalignment of the trenches. Thus the $\tilde{3} \rightarrow 1$ characteristics are slightly different from those measured in the $1 \rightarrow \tilde{3}$ configuration. As shown in the next section, this systematic asymmetry cancels out in all the eight states of the ORNAND gate.

The characteristics in Fig. 5 are taken at a constant positive collector bias $V_C = 2.3$ V in the operating regime of the device. As the heating voltage V_D increases, the channel current I_D first increases like in a field-effect transistor. When the V_D is high enough to establish a significant RST current, the I_D shows a negative differential resistance.[1] Prior to the onset of RST, the collector current is seen to decrease due to the reduction of leakage in the drain area with diminishing collector-to-drain bias.

Besides the electrical characteristic, Fig. 5 plots the luminescence power P_L measured with a broad-area Ge photodiode and suitable focusing optics. It is remarkable to note that prior to the onset of RST, there is virtually no light output, even though the collector current is nonnegligible. As discussed in detail in [11], this behavior is due to the fact that the leakage I_C^{LKC} is almost entirely formed by the emission of holes from the collector. Holes injected into the channel have a vastly lower radiative efficiency, because they are likely to reach a heavily doped contact before they recombine radiatively with electrons. In contrast, electrons injected into the collector are confined in the active region. Virtually all of the optical output can be attributed to the recombination of injected electrons in the collector active layer. The estimated internal radiative efficiency [11] at room temperature is approximately 5% for I_C^{RST} and only about 0.03% for I_C^{LKC}. At cryogenic temperatures, the radiative efficiency in the collector active layer increases to 30%.

[1]The peak-to-valley ratio in the negative differential resistance is not as high as that previously observed [14], [15] in unipolar charge injection transistors. This is due to a substantially higher doping in the emitter channel of the present device. The complementary nature of the collector by itself does not have a significant effect on the channel characteristics, provided the latter are measured at the same *electric field* in the collector barrier, i.e., apart from a trivial field-effect threshold shift.

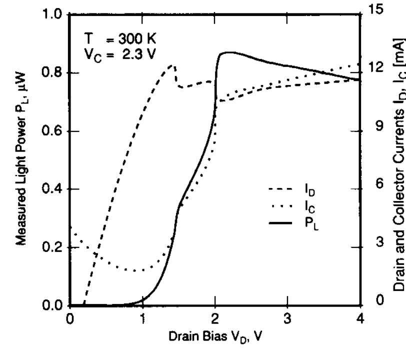


Fig. 5. Room-temperature current–voltage [$I_C(V_D)$ and $I_D(V_D)$] and light-voltage [$P_L(V_D)$] characteristics of a single-channel $\tilde{3} \rightarrow 1$ at a fixed collector bias $V_C = 2.3$ V. Electrode $\tilde{3}$ is grounded and 1 acts as the drain. Electrodes 2 and 3 are kept floating.

Single-channel characteristics of present devices are significantly improved over those reported earlier [11]. The key improvement lies in the larger I_C^{RST}, which is moreover achieved at lower V_C. This improvement can be attributed to a reduction of parasitic resistances. The present device, because of its multiterminal nature, naturally lends itself to a measurement of the series resistance R in electrodes 1 and 2. We have found $R = (10 \pm 1)\ \Omega$, dominated by the contact resistance. The outer electrodes can be expected to have slightly lower R.

The effect of adding external series resistances is illustrated in Fig. 6. Resistors in series with the source or the collector have a similar effect: its voltage drop effectively reduces the collector-to-source bias. The latter affects the normal electric field in the barrier and the sheet carrier concentration in the channel. A drain series resistance, on the other hand, reduces only the lateral channel field with the effect that the same I_C is reached at a higher V_D.

Fig. 7 shows the collector leakage current at $V_D = 0$. This experiment repeats that discussed in detail in our earlier report [11]. At low values of V_C in the forward direction and high enough temperatures ($T \gtrsim 250$ K) the I_C^{LKG} is almost entirely due to a thermionic emission of holes from the collector. The barrier height relative to the hole Fermi level is $\Phi_h = 0.92$ eV—calculated assuming the InGaAs energy gap $E_G = 0.75$ eV, the discontinuity $\Delta E_V = 0.2$ eV, and the given doping levels. On the other hand, the activation energy, determined from the temperature dependence of I_C extrapolated to $V_C \rightarrow 0$, corresponds to $\Phi_h = 0.84$ eV. This discrepancy is larger than that found earlier [11]; nevertheless, it is still within the margin of error due to possible deviations of the actual doping levels from nominal.

Fig. 8 reports a new and interesting finding which deserves further study. It shows the current–voltage characteristics for a grounded collector, both at 300 and 6 K. The built-in electric field at $V_C = 0$ opposes the RST of channel electrons and increases the effective barrier height, cf. Fig. 4(a). For $V_D > 0$, the device cross section near the drain is a reverse-biased p-n heterojunction. One would expect the characteristics to be similar to those in

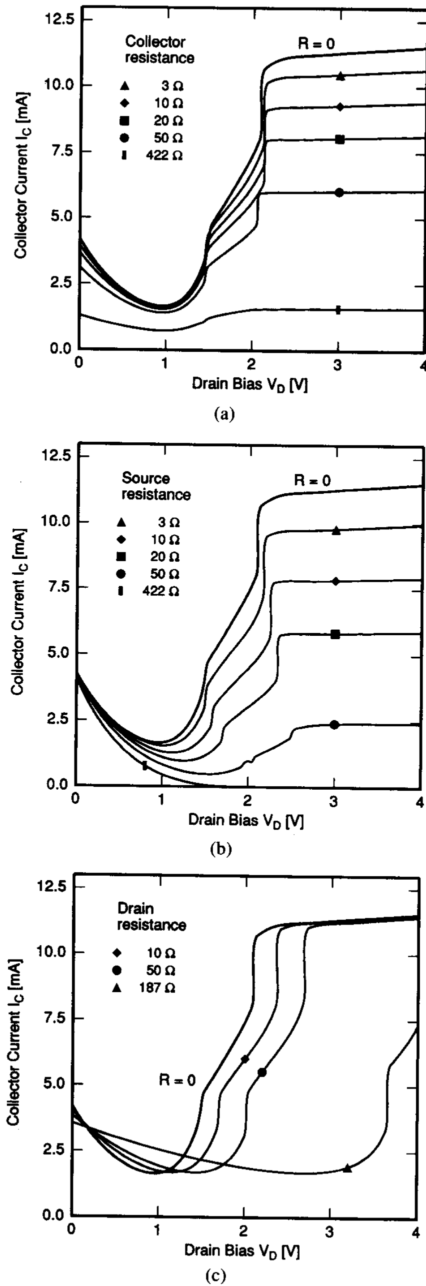


Fig. 6. The effect of series resistances. Current-voltage characteristics $I_C(V_D)$ of a single channel $\bar{3} \rightarrow 1$ measured under the same conditions as in Fig. 5 (though in a different device) with series resistances R added in (a) the collector, (b) the source, and (c) the drain circuits.

Fig. 7 for the reverse collector biases $V_C < 0$. However, at a certain drain bias, the curves $I_C(V_D)$ in Fig. 8(a) depart from the reverse-bias leakage curves, with the current increasing by several orders of magnitude. Such a regime had not been observed in our earlier studies [10], [11] where the emitter doping was lower and the channel was "normally-off," so that the transport properties at

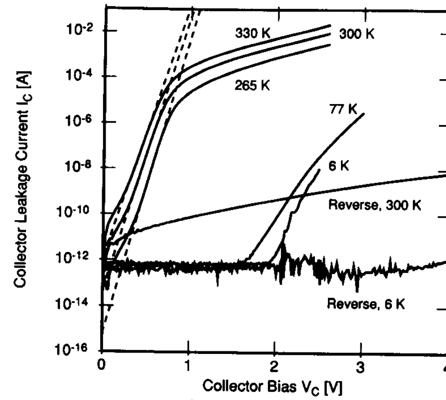


Fig. 7. Collector leakage current characteristics $I_C(V_C)$ at different temperatures, measured with all four emitter electrodes grounded. Forward-biased collector-emitter p-n junction corresponds to $V_C > 0$. The leakage current under reverse bias is of opposite polarity and the plotted curves represent $|I_C|$. Dashed lines indicate a linear extrapolation of log I_C to zero forward bias; temperature dependence of the extrapolated value gives an activation energy 0.84 eV.

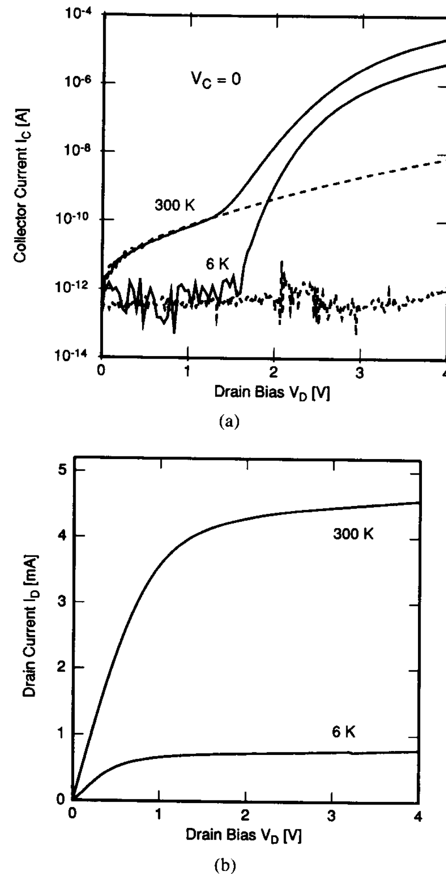


Fig. 8. Anomalous current-voltage characteristics of a single channel $\bar{3} \rightarrow 1$ at $V_C = 0$ and two different temperatures. Electrodes 2 and 3 are floating. (a) Solid lines show $I_C(V_D)$ at $V_C = 0$. Polarity of I_C corresponds to the flow of holes from the channel into the collector. Dashed lines represent the reverse-bias collector leakage current from Fig. 7. The "soft breakdown" $V_D \approx 1.5$ V is attributed to the RST of impact-ionized holes. (b) Drain characteristics $I_D(V_D)$ of the "normally-on" device.

$V_C = 0$ could not be properly investigated. Channel characteristics of the present device, Fig. 8(b), closely resemble those in a normally-on field-effect transistor and show no particular structure in the anomalous region.

We attribute the sharp rise of the reverse collector current (polarity corresponding to electrons flowing from the collector into the channel) at high values of $V_D \gtrsim 1.5$ V to the effect of *impact ionization* by hot electrons in the channel. Holes, released by this process near the drain, drift toward the source and undergo a substantial heating along the way. The observed increase of $|I_C|$ is thus interpreted as a RST of *minority holes* from the channel. Note that the same electric field that suppresses the RST of electrons aids the RST of channel holes. Obviously, this process leads to an injection of *majority* carriers into the collector and does not give rise to a luminescence—which is in accordance with our experimental observations. At cryogenic temperatures, the ionization threshold in InGaAs increases due to the bandgap widening and so does the critical value of V_D at which the $I_C(V_D)$ curves in Fig. 8(a) depart from the corresponding leakage curves. Evidently, the complementary structure is not essential, although it simplifies observation of the minority RST effect by reducing the leakage current under reverse bias. Similar effects have been seen in *unipolar* CHINT structures with a heavier than usual channel doping at low and *negative* collector biases [16]. The RST of minority carriers can be a powerful tool for studying impact ionization phenomena in field-effect transistor channels.

IV. Logic

Since we set the periodic boundary conditions $V_{\tilde{3}} = V_3$, our multiterminal device has effectively three input terminals. One of these can be viewed as a control electrode which determines which of the two logic function **or** or **nand** is executed on the other two inputs. Choice of the control electrode is arbitrary. The collector current I_C and the light power P_L represent the logic output. We shall refer to the states with *high* and *low* values of the output as *on* and *off* states, respectively.

Fig. 9 demonstrates the room-temperature logic operation of our multiterminal device. The light signal has been detected from the back of the polished substrate using a microscope objective to collect the light. The substrate thickness has been polished down to 35 μm reducing the free carrier absorption in the substrate. The collector bias is fixed at $V_C = 2.4$ V and the input signals V_1 and V_2 are varied between *low* = 0 and *high* = 3 V, while the split electrode, chosen as the control, is fixed either at the *low* value $V_3 = 0$ for the **or** function or at the *high* value $V_3 = 3$ V for the **nand** function.

As seen from Fig. 9, the symmetry between different *on* states is well maintained, both for $I_C(\pm 8\%)$ and $P_L(\pm 6\%)$. The larger variation in I_C is due to the variation in the leakage current of holes. Different *on* states correspond to different areas A_S of the source contact: A_S is 25% of the total emitter area of **nand**(0,1) and **nand**(1,0),

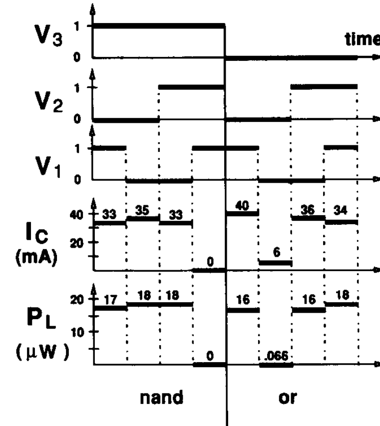
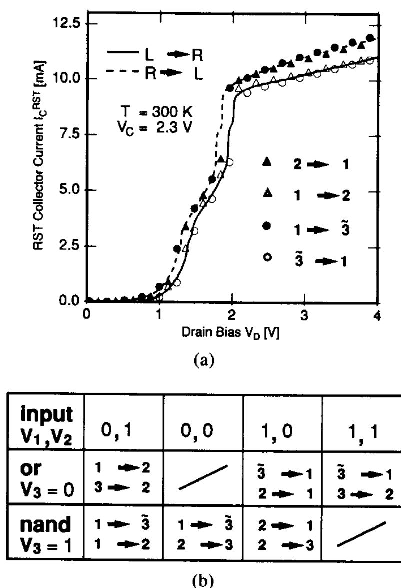


Fig. 9. Optical and electrical logic operation of the ORNAND gate, obtained in a quasi-stationary measurement at room temperature and V_C = 2.4 V. Electrodes 3 and $\tilde{3}$ are tied together. The binary values "logic-0" and "logic-1" of the input signals V_1, V_2, and V_3 correspond to 0 and 3 V, respectively. The particular grouping of the states into OR and NAND reflects the choice of V_3 as the "control" electrode.

while A_S = 75% for **or**(0,1) and **or**(1,0), and A_S = 50% for **nand**(0,0) and **or**(1,1). The larger the source area the larger is the leakage current which is added to the RST current. Since the radiative efficiency of I_C^{LKC} is negligible compared to that of I_C^{RST}, the *on* states are more homogeneous in the measured light output. The low radiative efficiency of I_C^{LKG} also explains the fact that the *off* state of the **or** function is less satisfactory electrically (the room-temperature *on*/*off* ratio $\approx$ 7 in I_C) than optically (*on*/*off* $\gtrsim$ 200 in P_L). In the *off* state there is no RST and most of leakage results from holes injected in the emitter layer.[2]

Variation in the effective source area is not the only cause for violation of the basic symmetry (1). In principle, the symmetry between different *on* states may be broken by a leakage along the mesa sidewall, which should have no effect, however, on the optical logic performance. Another way to break this symmetry is to displace the channel-defining trench in the n^+ cap layer from its nominal position exactly in the middle between neighboring electrodes. Fig. 10(a) shows the single-channel $I_C^{\mathrm{RST}}(V_D)$ characteristics for two different channels and two different source $\rightarrow$ drain orientations. We see that the curves corresponding to the same orientation in two different channels coincide more closely than those for the same channel but different orientations. This observation holds true for all devices examined. We remark that the data in the present report have been collected from a wafer with an exceptionally lucky alignment of the trench and the source/drain metal masks. In other wafers, the difference between the RST in opposite orientations of the same channel is even larger. Nevertheless, this has no effect on the symmetry of *on* states in the ORNAND gate. Indeed,

[2]The electrical logic operation is a significant improvement over our previous report [11] where the output-current logic-*off* state was washed out at room temperature by the parasitic leakage of holes.



(a)

input V_1, V_2	0, 1	0, 0	1, 0	1, 1
or $V_3 = 0$	1 → 2 3 → 2	/	$\tilde{3}$ → 1 2 → 1	$\tilde{3}$ → 1 3 → 2
nand $V_3 = 1$	1 → $\tilde{3}$ 1 → 2	1 → $\tilde{3}$ 2 → 3	2 → 1 2 → 3	/

(b)

Fig. 10. Asymmetry due to the misalignment of trenches in the ORNAND gate of Fig. 3. The arrow indicates the source → drain orientation and its position the trench misalignment. Thus the symbol $S + \rightarrow D$ indicates that the trench is closer to the drain (D) electrode. (a) Comparison of the RST for two opposite orientations of the channel field in two different channels. The leakage current I_C^{LKG} is subtracted, as in [11]. (b) Table of the channels under the heating field ("working channels") in all logic states of the gate.

the symmetry break due to a trench misalignment has to be identical in all the three channels, cf. Fig. 3. Noting that each of the six *on* states has two channels under field—one of each orientation—we see that the systematic asymmetry cancels out in the ORNAND logic operation, cf. the table in Fig. 10(b).

V. Conclusion

A monolithic multiterminal logic device, that functions both optically and electrically as an ORNAND gate, has been demonstrated for the first time. The device, based on the real-space transfer of hot electrons into a complementary collector layer is implemented in an InGaAs/InAlAs/InGaAs heterstructure. The collector current and the optical output power both exhibit the **or** and the **nand** functions of any two of the three input terminals. These functions are not fixed by the layout but are interchangeable by the voltage on the third ("control") terminal. Choice of the control electrode is, moreover, arbitrary. This is the first implementation of a single logic device with such powerful capabilities; its function is electrically reprogrammable in the course of a circuit operation.

In the heterostructure used the valence-band discontinuity is much smaller than that in the conduction band and most of the parasitic non-RST current is due to the injection of holes from the p-type collector layer into the n-type emitter. Due to a specially designed collector structure with a wide-gap InAlAs layer confining the active InGaAs layer, the radiative efficiency of minority carriers in the collector is much higher than that in the emitter. This makes the leakage current relatively nonradiative and substantially enhances the optical logic performance at room temperature.

The demonstrated device is an incoherent light-emitting source, similar to a conventional LED. In order to increase its output power and improve the frequency performance, we must take advantage of the stimulated emission in a resonant optical cavity. The high injection current density, $J_C \gtrsim 25\ \text{kA/cm}^2$, obtained in the present device is promising for the future realization of a real-space transfer logic laser. However, the implementation of a laser will require an improvement in the internal radiative efficiency. This can be accomplished by an optimized structure design—similar to that currently employed in heterostructure lasers—with a lower doping levels both in the active region and the confinement layer.

References

[1] S. Luryi, A. Kastalsky, A. C. Gossard, and R. H. Hendel, "Charge injection transistor based on real space hot-electron transfer," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 832–839, 1984.

[2] Z. S. Gribnikov, "Negative differential conductivity in a multilayer heterostructure," *Fiz. Tekh. Poluprovodn.*, vol. 6, p. 1380, 1972 (*Sov. Phys.—Semicond.*, vol. 6, p. 1204, 1973).

[3] K. Hess, H. Morkoç, H. Shichijo, and B. G. Streetman, "Negative differential resistance through real-space electron transfer," *Appl. Phys. Lett.*, vol. 35, p. 469, 1979.

[4] S. Luryi and A. Kastalsky, "Hot electron injection devices," *Superlatt. Microstr.*, vol. 1, pp. 389–400, 1985.

[5] A. Kastalsky, "Novel real-space transfer devices," in *High-Speed Electronics*, B. Kallback and H. Beneking, Eds. Berlin: Springer-Verlag, 1986, pp. 62–71.

[6] S. Luryi, P. Mensz, M. Pinto, P. A. Garbinski, A. Y. Cho, and D. L. Sivco, "Charge injection logic," *Appl. Phys. Lett.*, vol. 57, pp. 1787–1789, 1990.

[7] S. Luryi, "Light emitting devices based on the real-space-transfer of hot electrons," *Appl. Phys. Lett.*, vol. 58, pp. 1727–1729, 1991.

[8] H. Tian, K. W. Kim, and M. A. Littlejohn, "Novel heterojunction real-space transfer logic transistor structures: A model-based investigation," *IEEE Trans. Electron Devices*, vol. 39, pp. 2189–2196, 1992.

[9] P. M. Mensz, A. Y. Cho, and D. L. Sivco, "Charge injection frequency multiplier," *Appl. Phys. Lett.*, vol. 61, pp. 934–936, 1992.

[10] M. Mastrapasqua, F. Capasso, S. Luryi, A. L. Hutchinson, D. L. Sivco, and A. Y. Cho, "Light emitting charge injection transistor with p-type collector," *Appl. Phys. Lett.*, vol. 60, pp. 2415–2417, 1992.

[11] M. Mastrapasqua, S. Luryi, F. Capasso, A. L. Hutchinson, D. L. Sivco, and A. Y. Cho, "Light emitting transistor based on real-space transfer: Electrical and optical properties," *IEEE Trans. Electron Devices*, vol. 40, pp. 250–258, 1993.

[12] S. Luryi and M. R. Pinto, "Broken symmetry and the formation of hot-electron domains in real-space transfer transistors," *Phys. Rev. Lett.*, vol. 67, pp. 2351–2354, 1991.
—, "Symmetry of the real-space transfer and collector-controlled states in charge injection transistors," *Semicond. Sci. Tech.*, vol. 7, pp. B520–B526, 1992.

[13] M. Pinto and S. Luryi, "Simulation of multiply connected current-voltage characteristics in charge injection transistors," in *IEDM Tech. Dig.*, 1991, pp. 507–510.

[14] P. M. Mensz, S. Luryi, A. Y. Cho, D. L. Sivco, and F. Ren, "Real space transfer in three-terminal InGaAs/InAlAs/InGaAs heterostructure devices," *Appl. Phys. Lett.*, vol. 56, pp. 2563–2565, 1990.

[15] P. M. Mensz, P. A. Garbinski, A. Y. Cho, D. L. Sivco, and S. Luryi, "High transconductance and large peak-to-valley ratio of negative differential conductance in three-terminal InGaAs/InAlAs real-space transfer devices," *Appl. Phys. Lett.*, vol. 57, pp. 2558–2560, 1990.

[16] G. L. Belenky and S. Luryi, unpublished.

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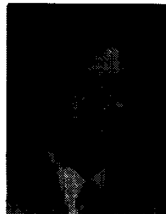
G. L. Belenky, photograph and biography not available at the time of publication.

P. A. Garbinski, photograph and biography not available at the time of publication.



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He is Director of the Materials Processing Research Laboratory at AT&T Bell Laboratories, Murray Hill, NJ. He joined Bell Laboratories in 1968 where he developed a crystal growth technology called molecular-beam epitaxy (MBE). His many significant research accomplishments include the construction of surface phase diagram for MBE crystal growth, the first fabrication of an MBE artificial superlattice, the first MBE IMPATT diode, mixer diode, and field-effect transistor operating at microwave frequencies, and the first MBE double-heterostructure laser operating CW at room temperature. His recent work is in the area of quantum-well devices. He has published over 250 papers in surface physics, crystal growth, and device physics and performance. He holds 43 patents on crystal growth and semiconductor devices related to MBE.

Dr. Cho is a recipient of the Electronics Division Award of the Electrochemical Society (1977), the American Physical Society International Prize for New Materials (1982), the IEEE Morris N. Liebmann Award (1982), the University of Illinois Electrical and Computer Engineering Distinguished Alumnus Award (1985), the Chinese Institute of Engineers USA Distinguished Achievement Award (1985), the GaAs Symposium Award-Ford (1986), the Heinrich Welker Medal-Siemens (1986), the Solid State Science and Technology Medal of the Electrochemical Society (1987), the College of Engineering Alumni Honor Award of the University of Illinois (1988), the World Materials Congress Award of ASM International (1988), the Gaede-Langmuir Award of the American Vacuum Society (1988), and the Industrial Research Institute Achievement Award of the Industrial Research Institute, Inc. (1988). He is a Fellow of the American Physical Society, and the American Academy of Arts and Sciences. He is a member of the American Vacuum Society, the Electrochemical Society, the Materials Research Society, the National Academy of Engineering, and the National Academy of Sciences.

Deborah L. Sivco, photograph and biography not available at the time of publication.